EE 508

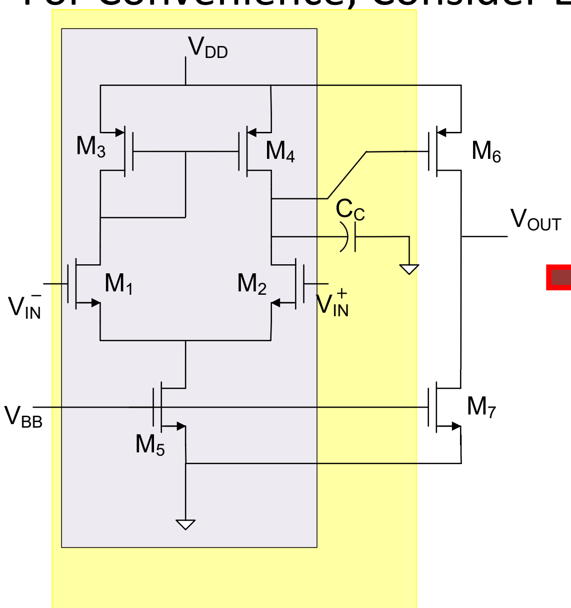
Lecture 43

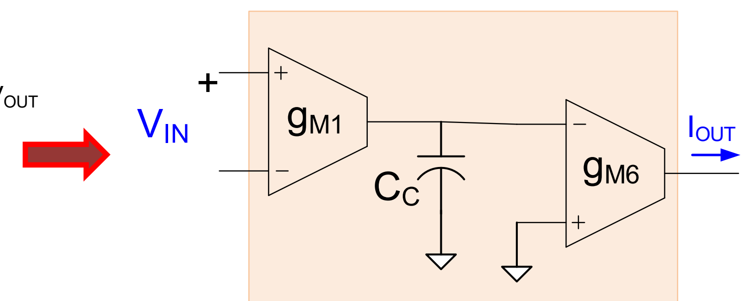
Basic Filter Components

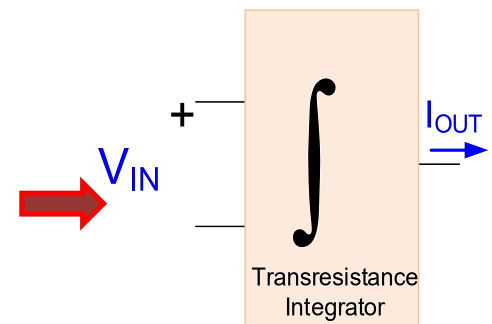
- All Pass Networks
- Arbitrary Transfer Function Synthesis
- Impedance Transformation Circuits
- Equalizers

Towards Active R Filters

For Convenience, Consider Externally Compensated 7T Op Amp







If M3:M4 gain =1

$$\frac{I_{OUT}}{V_{IN}} = -\frac{I_O}{s}$$

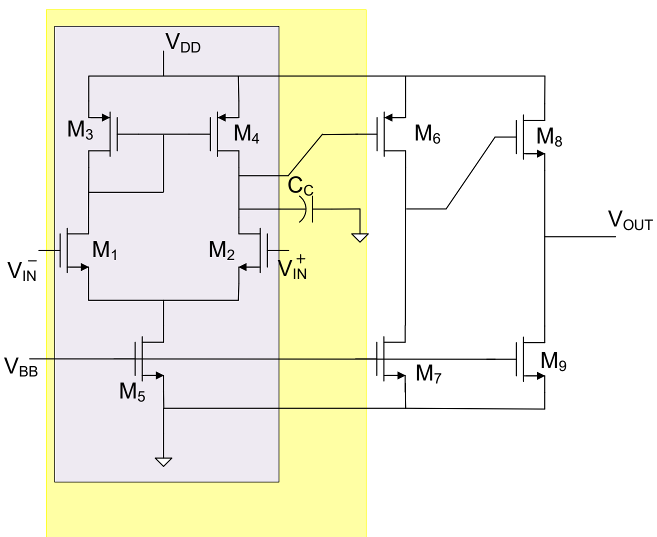
$$I_{OUT} = -\frac{g_{m1}g_{m6}}{sC_C}$$

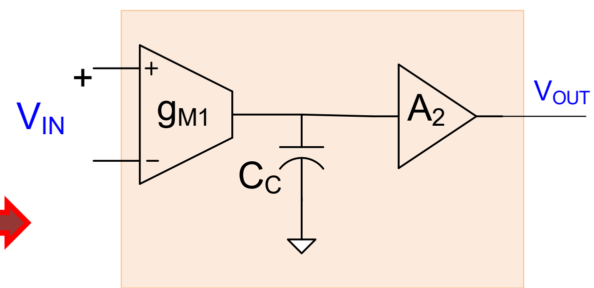
$$I_{OUT} = -\frac{g_{m1}g_{m6}}{sC_C}$$

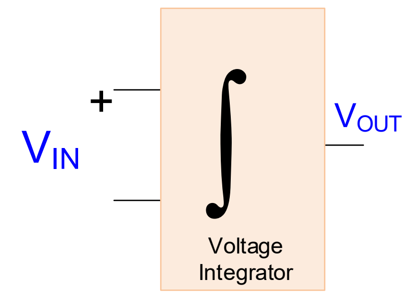
- Behaves as Transresistance Integrator !
- Though the first commercial OTA was introduced in late 1960’s the use of OTAs to design filters received almost no attention for almost 15 years
- Concept developed for a two-stage externally compensated op amp, basic properties exist for most high output impedance op amps

Towards Active R Filters

For Convenience, Consider Externally Compensated 9T Op Amp







$$A_2 = -\frac{g_{m6}}{g_{O6}+g_{O7}}$$

If M3:M4 gain =1

$$V_{OUT} = \frac{A_2 g_{m1}}{sC_C} V_{IN}$$

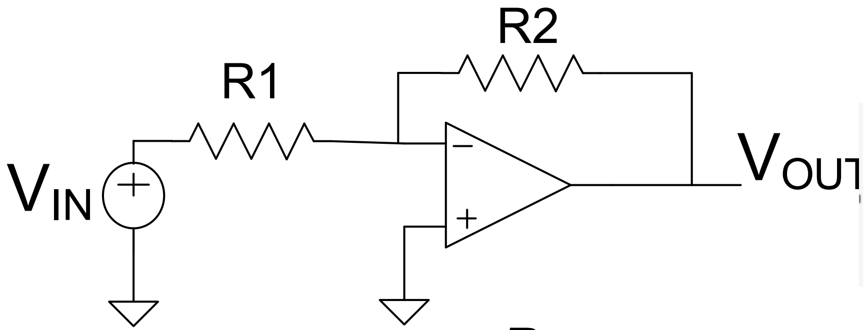
$$I_O = -\frac{A_2 g_{m1}}{sC_C}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{I_O}{s}$$

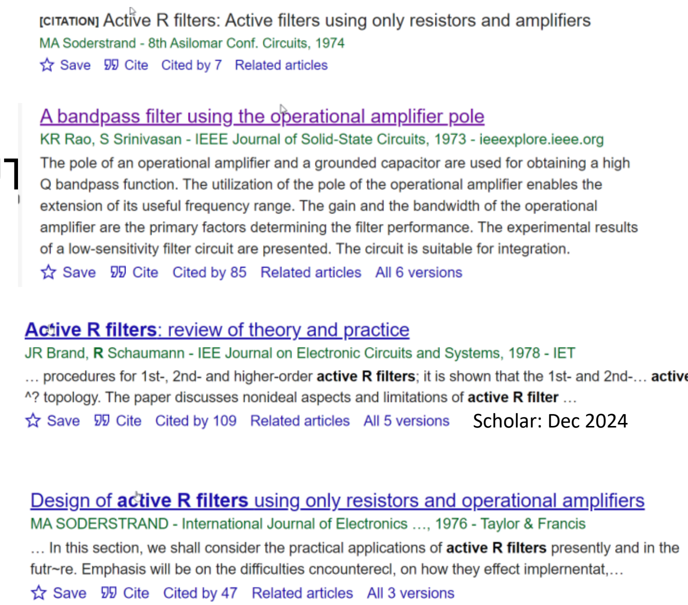
$$I_O = -\frac{A_2 g_{m1}}{sC_C}$$

- Behaves as Voltage Integrator !
- Though concept developed for a two-stage externally compensated op amp, basic properties exist for most low output impedance op amps

Amplifier or LP Filter or Lossy Integrator?



$$\frac{V_{OUT}}{V_{IN}} \cong \frac{-\frac{R_2}{R_1}}{1+\tau s\left(1+\frac{R_2}{R_1}\right)}$$


[CITATION] Active R filters: Active filters using only resistors and amplifiers
MA Soderstrand - 8th Asilomar Conf. Circuits, 1974
Save Cite Cited by 7 Related articles

A bandpass filter using the operational amplifier pole
KR Rao, S Srinivasan - IEEE Journal of Solid-State Circuits, 1973 - ieeexplore.ieee.org
The pole of an operational amplifier and a grounded capacitor are used for obtaining a high Q bandpass function. The utilization of the pole of the operational amplifier enables the extension of its useful frequency range. The gain and the bandwidth of the operational amplifier are the primary factors determining the filter performance. The experimental results of a low-sensitivity filter circuit are presented. The circuit is suitable for integration.
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Active R filters: review of theory and practice
JR Brand, **R** Schaumann - IEE Journal on Electronic Circuits and Systems, 1978 - IET
… procedures for 1st-, 2nd- and higher-order **active R filters**; it is shown that the 1st- and 2nd-… **active** ^? topology. The paper discusses nonideal aspects and limitations of **active R filter** …
Save Cite Cited by 109 Related articles All 5 versions

Design of **active R filters** using only resistors and operational amplifiers
MA SODERSTRAND - International Journal of Electronics …, 1976 - Taylor & Francis
… In this section, we shall consider the practical applications of **active R filters** presently and in the futr~re. Emphasis will be on the difficulties cncounterecl, on how they effect inplementat,…
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Scholar: Dec 2024

- In about 1974 Michael Soderstrand introduced this concept for building high-frequency filters and termed these “Active-R” filters

- Concept of incorporating op amp pole in determining filter response reported a bit earlier

- The compensation capacitor in the op amp serves as the energy storage element in the filter

- Can operate at very high frequencies but many problems with linearity and accuracy

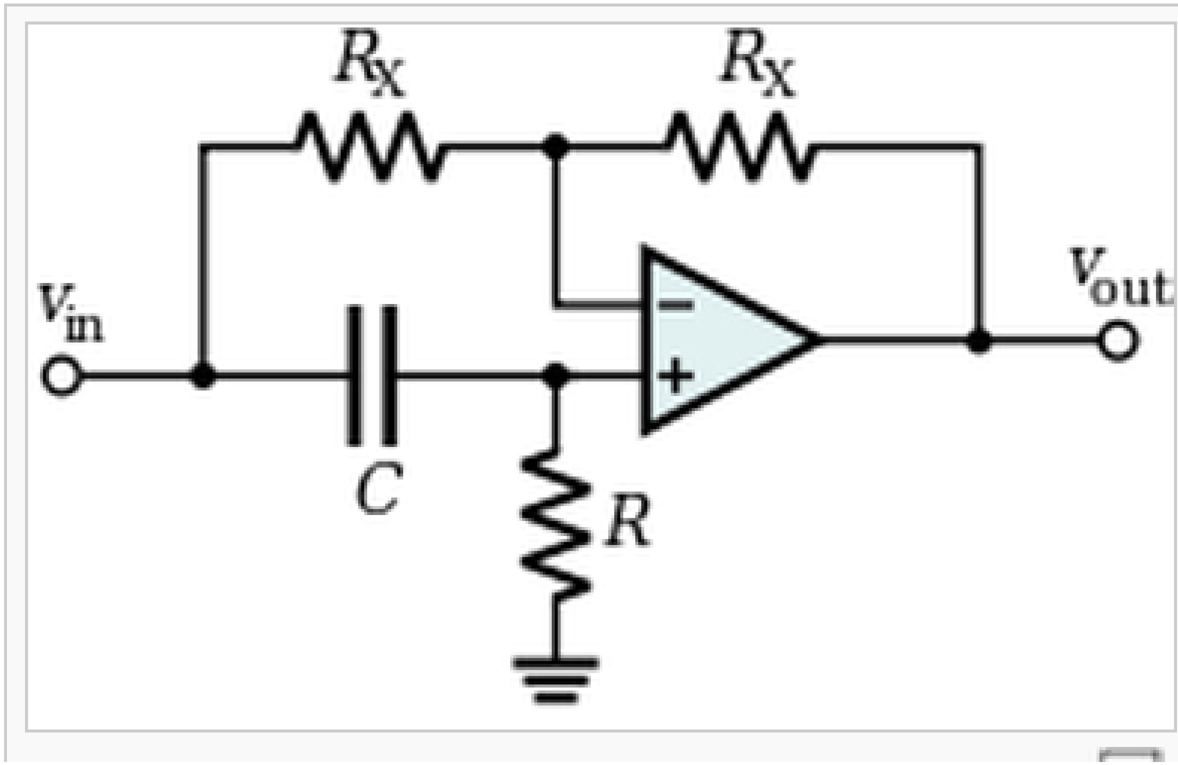
Basic Filter Components

- All Pass Networks
- Arbitrary Transfer Function Synthesis
- Impedance Transformation Circuits
- Equalizers

All-Pass Circuits

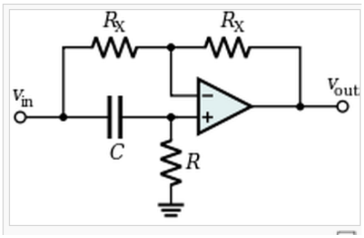
- Magnitude of Gain is Constant
- Phase Changes with Frequency
- Used to correct undesired phase characteristics of a filter

First-Order All Pass

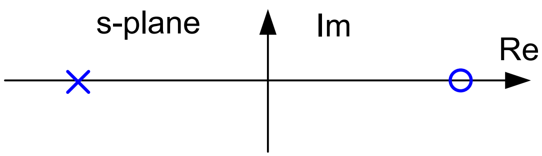


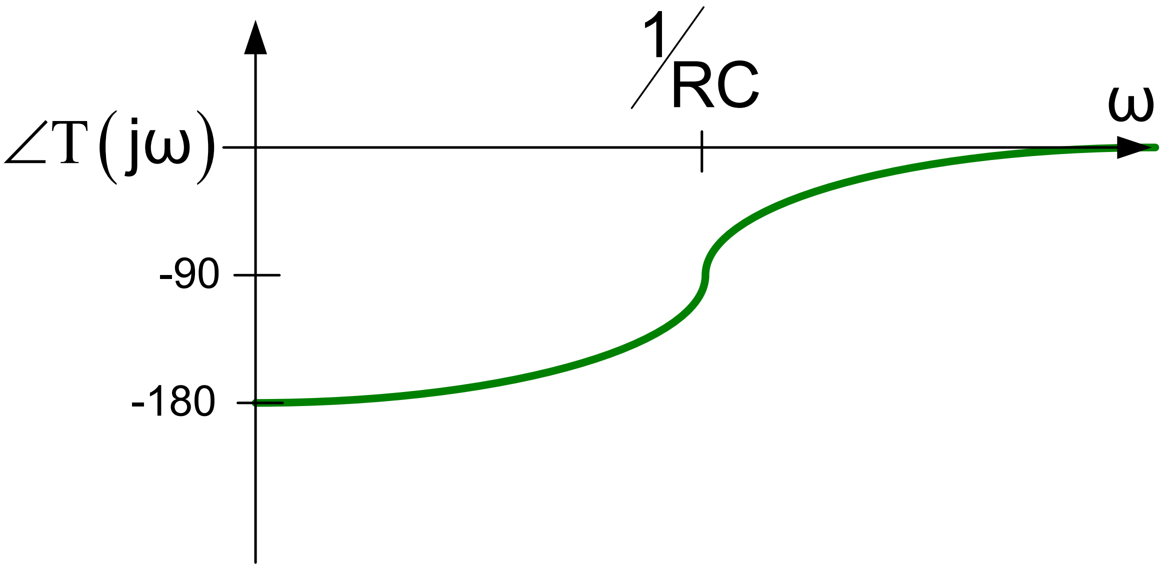
$$T(s) = \frac{s - \frac{1}{RC}}{s + \frac{1}{RC}}$$

First-Order All Pass

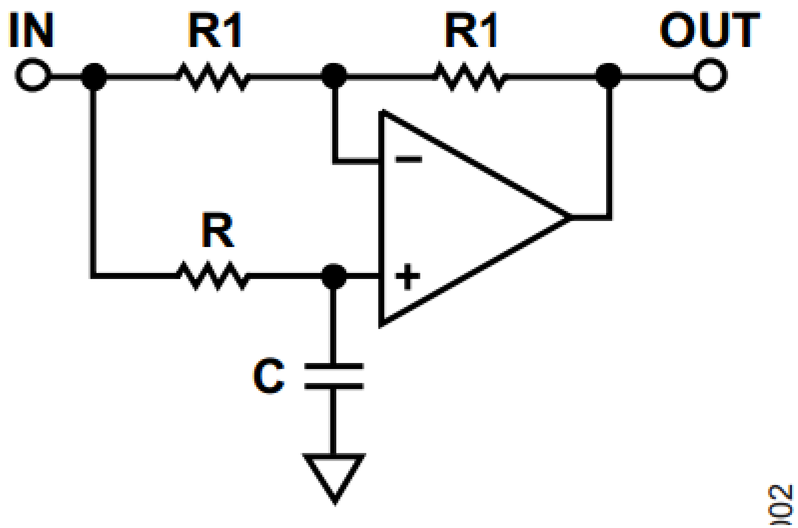


$$T(s) = \frac{s - \frac{1}{RC}}{s + \frac{1}{RC}}$$



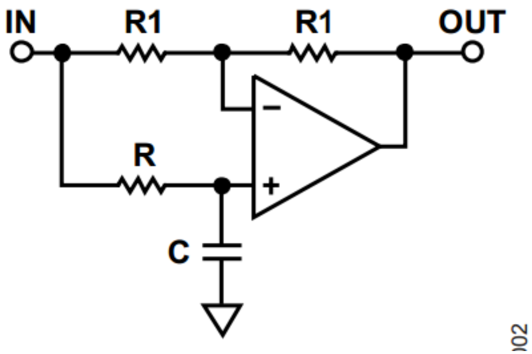


First-Order All Pass

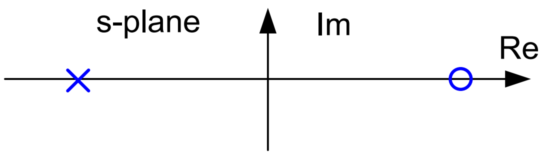


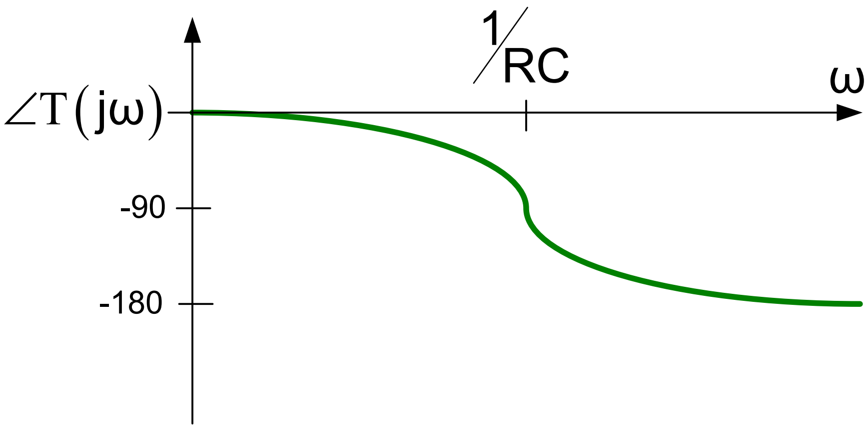
$$T(s) = -\frac{s - \frac{1}{RC}}{s + \frac{1}{RC}}$$

First-Order All Pass

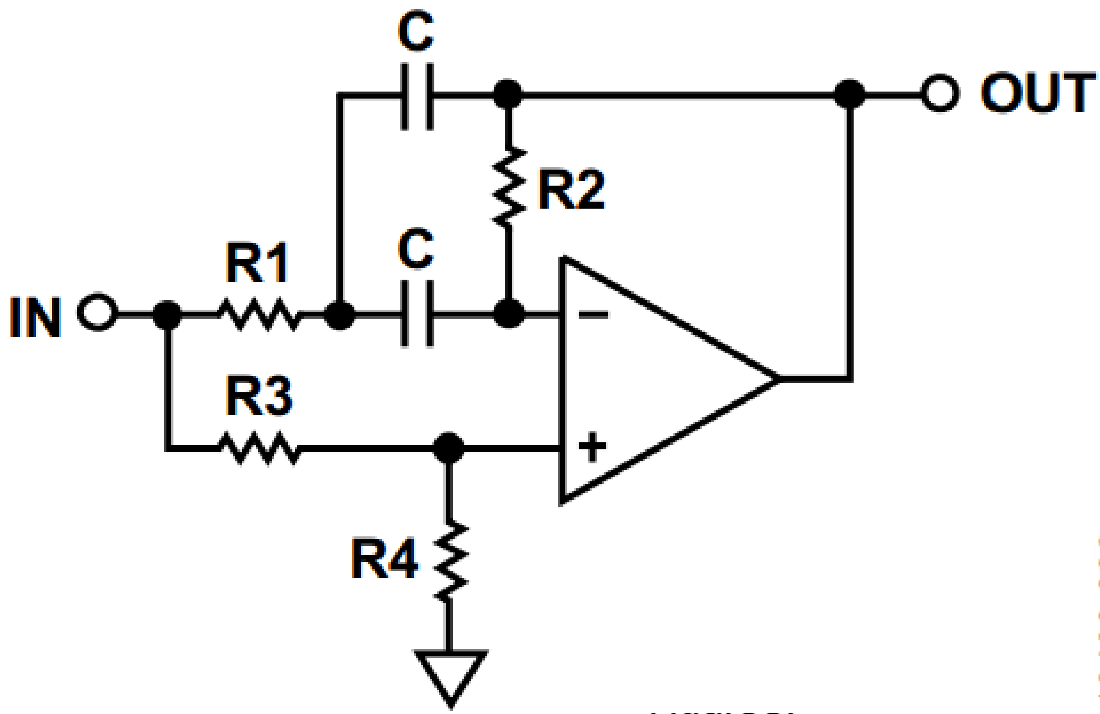


$$T(s) = -\frac{s - \frac{1}{RC}}{s + \frac{1}{RC}}$$





Second-Order All Pass

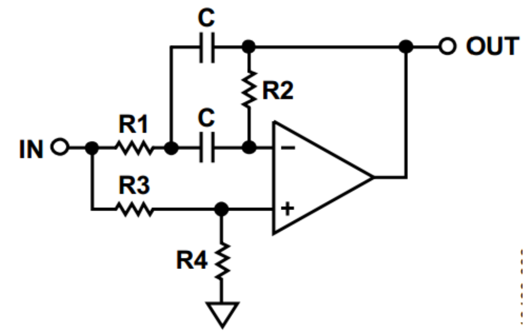


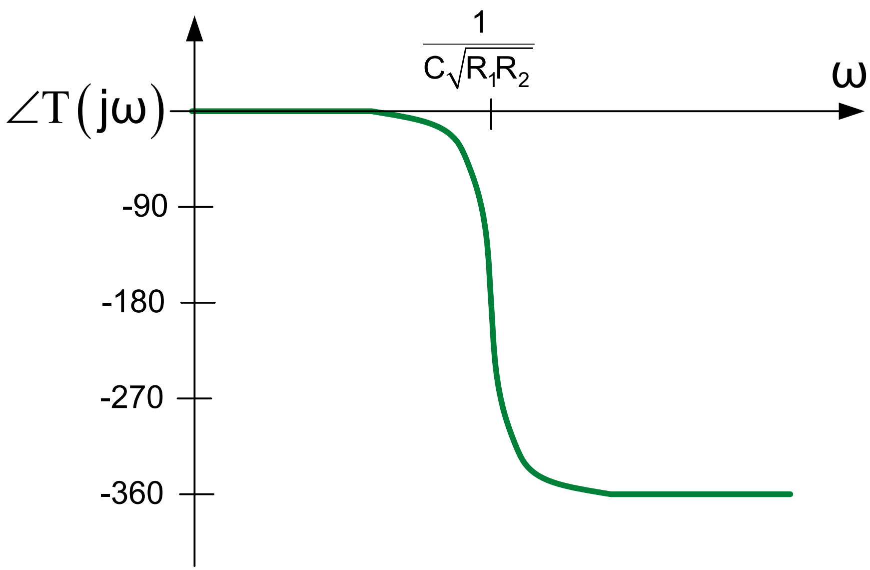
$$\frac{V_O}{V_{IN}} = \frac{s^2 - s\left(\frac{2}{R2\,C}\right) + \frac{1}{R1\;R2\;C^2}}{s^2 + s\left(\frac{2}{R2\,C}\right) + \frac{1}{R1\;R2\;C^2}}$$

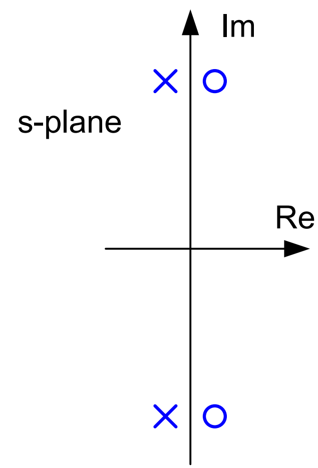
Based upon Bridged-T Feedback Structure

Second-Order All Pass

$$\frac{V_O}{V_{IN}} = \frac{s^2 - s\left(\frac{2}{R2\,C}\right) + \frac{1}{R1\;R2\;C^2}}{s^2 + s\left(\frac{2}{R2\,C}\right) + \frac{1}{R1\;R2\;C^2}}$$







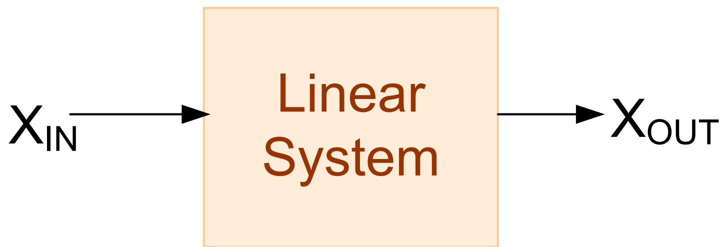
Basic Filter Components

- All Pass Networks
- Arbitrary Transfer Function Synthesis
- Impedance Transformation Circuits
- Equalizers

Arbitrary Transfer Function Synthesis

- Based upon coefficient derivation
- Can be used to implement/solve an arbitrary differential equation
- Versatile
- Basic concept of Analog Computer

Applications of integrators to solving differential equations



Standard Integral form of a differential equation

$$X_{OUT} = b_1 \int X_{OUT} + b_2 \iint X_{OUT} + b_3 \iiint X_{OUT} + \ldots + a_0 X_{IN} + \int X_{IN} + \iint X_{IN} + \ldots$$

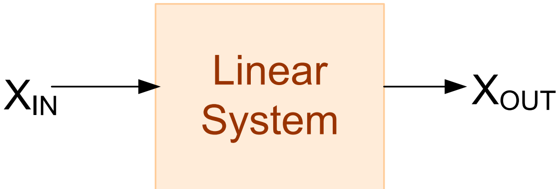
Standard differential form of a differential equation

$$X_{OUT} = \alpha_1 X_{OUT}^{'} + \alpha_2 X_{OUT}^{''} + \alpha_3 X_{OUT}^{'''} + \ldots + \beta_1 X_{IN} + \beta_2 X_{IN}^{'} + \beta_3 X_{IN}^{''} + \ldots$$

Initial conditions not shown

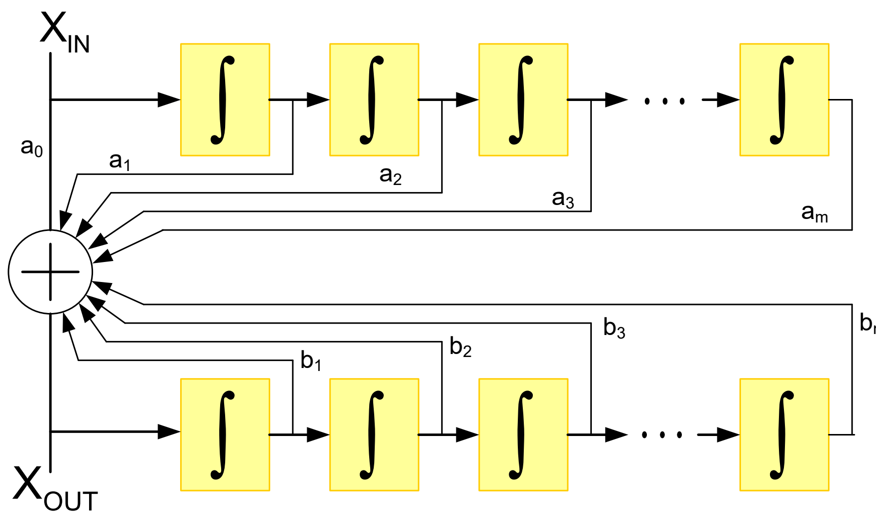
Can express any system in either differential or integral form

Applications of integrators to solving differential equations



Consider the standard integral form

$$X_{OUT} = b_1 \int X_{OUT} + b_2 \iint X_{OUT} + b_3 \iiint X_{OUT} + \ldots + a_0 X_{IN} + \int X_{IN} + \iint X_{IN} + \ldots$$



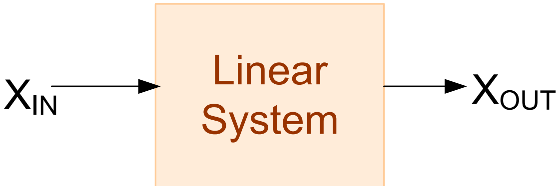
One Implementation (direct and intuitive)

This circuit is comprised of summers and integrators

Can solve an arbitrary linear differential equation

This concept was used in Analog Computers in the past

Applications of integrators to solving differential equations



Consider the standard integral form

$$X_{OUT} = b_1 \int X_{OUT} + b_2 \iint X_{OUT} + b_3 \iiint X_{OUT} + \ldots + a_0 X_{IN} + \int X_{IN} + \iint X_{IN} + \ldots$$

Take the Laplace transform of this equation

$$\mathcal{X}_{OUT} = b_1 \frac{1}{s} \mathcal{X}_{OUT} + b_2 \frac{1}{s^2} \mathcal{X}_{OUT} + b_3 \frac{1}{s^3} \mathcal{X}_{OUT} + \ldots + b_n \frac{1}{s^n} + a_0 \mathcal{X}_{IN} + a_1 \frac{1}{s} \mathcal{X}_{IN} + a_2 \frac{1}{s^2} \mathcal{X}_{IN} + a_3 \frac{1}{s^3} \mathcal{X}_{IN} + \ldots + a_m \frac{1}{s^m}$$

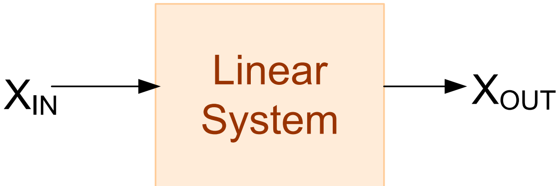
Multiply by s^n and assume m=n (some of the coefficients can be 0)

$$s^n \mathcal{X}_{OUT} = b_1 s^{n-1} \mathcal{X}_{OUT} + b_2 s^{n-2} \mathcal{X}_{OUT} + b_3 s^{n-3} \mathcal{X}_{OUT} + \ldots + b_n + a_0 s^n \mathcal{X}_{IN} + a_1 s^{n-1} \mathcal{X}_{IN} + a_2 s^{n-2} \mathcal{X}_{IN} + a_3 s^{n-3} \mathcal{X}_{IN} + \ldots + a_n$$

$$\mathcal{X}_{OUT}\left(s^n - b_1 s^{n-1} - b_2 s^{n-2} - b_3 s^{n-3} - \ldots - b_n\right) = \mathcal{X}_{IN}\left(a_0 s^n + a_1 s^{n-1} + a_2 s^{n-2} + a_3 s^{n-3} + \ldots + a_n\right)$$

$$T(s) = \frac{\mathcal{X}_{OUT}}{\mathcal{X}_{IN}} = \frac{a_0 s^n + a_1 s^{n-1} + a_2 s^{n-2} + a_3 s^{n-3} + \ldots + a_n}{s^n - b_1 s^{n-1} - b_2 s^{n-2} - b_3 s^{n-3} - \ldots - b_n}$$

Applications of integrators to solving differential equations



Consider the standard integral form

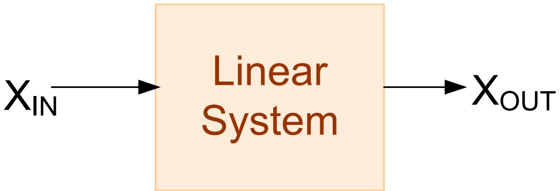
$$X_{OUT} = b_1 \int X_{OUT} + b_2 \iint X_{OUT} + b_3 \iiint X_{OUT} + \ldots + a_0 X_{IN} + \int X_{IN} + \iint X_{IN} + \ldots$$

$$T(s) = \frac{\mathcal{X}_{OUT}}{\mathcal{X}_{IN}} = \frac{a_0 \mathrm{s}^{n} + a_1 \mathrm{s}^{n-1} + a_2 \mathrm{s}^{n-2} + a_3 \mathrm{s}^{n-3} + \ldots + a_n}{\mathrm{s}^{n} - b_1 \mathrm{s}^{n-1} - b_2 \mathrm{s}^{n-2} - b_3 \mathrm{s}^{n-3} - \ldots - b_n}$$

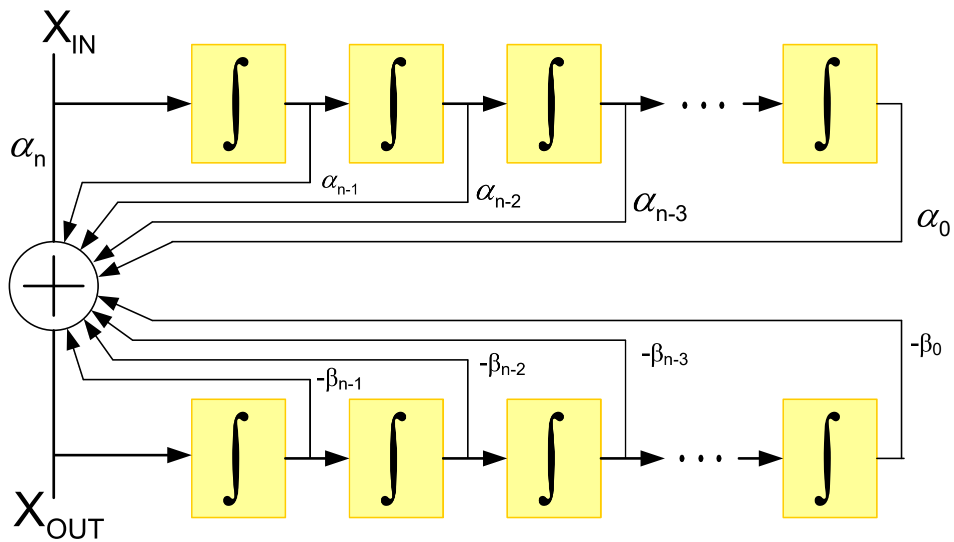
This can be written in more standard form

$$T(s) = \frac{\alpha_n \mathrm{s}^{n} + \alpha_{n-1} \mathrm{s}^{n-1} + \ldots \alpha_1 \mathrm{s} + \alpha_0}{\mathrm{s}^{n} + \beta_{n-1} \mathrm{s}^{n-1} + \ldots + \beta_1 \mathrm{s} + \beta_0}$$

Applications of integrators to filter design



$$T(s) = \frac{\alpha_n s^n + \alpha_{m-1} s^{n-1} + \ldots \alpha_1 s + \alpha_0}{s^n + \beta_{n-1} s^{n-1} + \ldots + \beta_1 s + \beta_0}$$



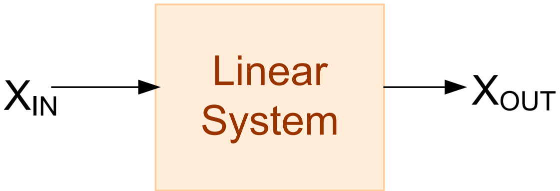
One Implementation (direct and intuitive)

Can design (synthesize) any T(s) with just integrators and summers !

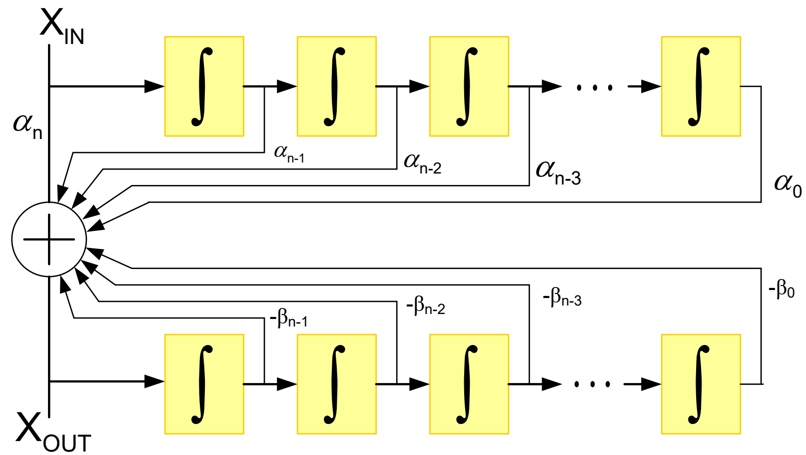
Integrators are not used “open loop” so loss is not added

Although this approach to filter design works, often more practical methods are used

Applications of integrators to filter design



$$T(s)=\frac{\alpha_n s^n+\alpha_{m-1}s^{n-1}+\ldots\alpha_1 s+\alpha_0}{s^n+\beta_{n-1}s^{n-1}+\ldots+\beta_1 s+\beta_0}$$



One Implementation (direct and intuitive)

What are some other architectural implementations?

Cascaded Biquads

Leapfrog

Though these other implementations may have better performance, not as easily programmable to realize different functions

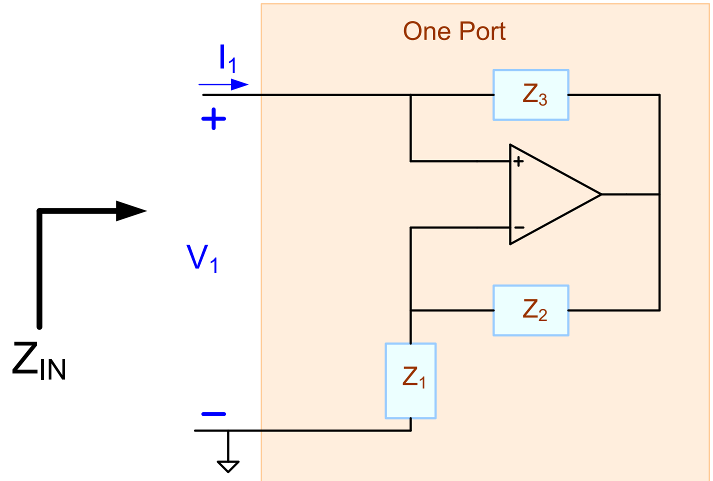
Basic Filter Components

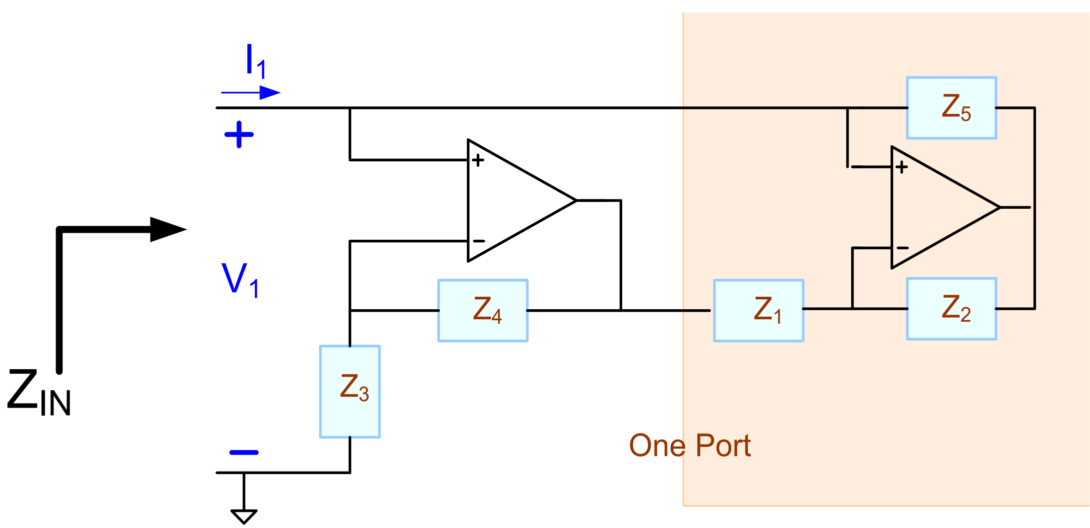
- All Pass Networks
- Arbitrary Transfer Function Synthesis
- Impedance Transformation Circuits
- Equalizers

Impedance Synthesis

- Focus on synthesizing impedance rather than transfer function
- Gyrators will provide inductance simulation
- Capacitance Multiplication
- Synthesis of super components

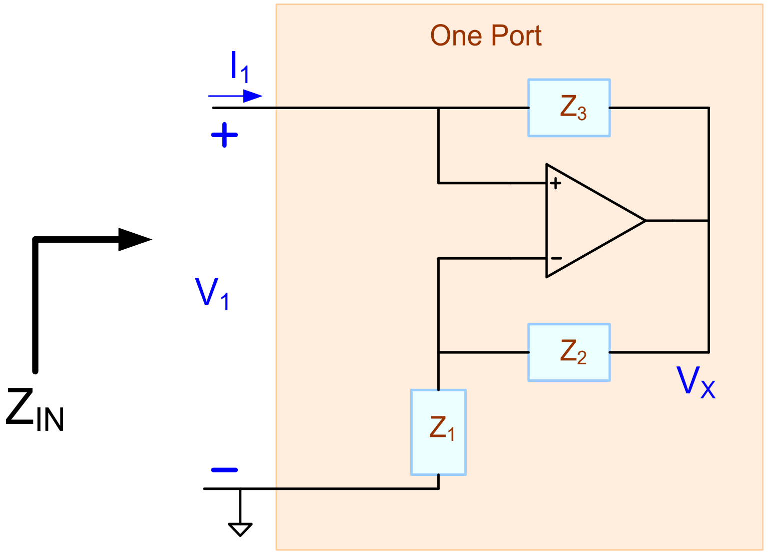
Impedance Converters





Note these circuits are strictly one-ports and have no output node

Impedance Converters



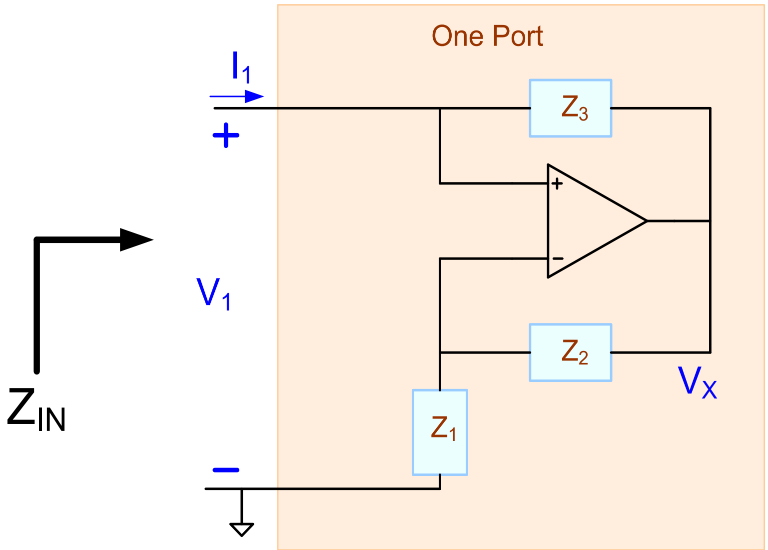
$$V_1(G_1+G_2) = V_X G_2$$

$$I_1=(V_1-V_X)G_3$$

$$Z_{IN} = -\frac{Z_1 Z_3}{Z_2}$$

Observe this input impedance is negative!

Impedance Converters



$$Z_{IN} = -\frac{Z_1 Z_3}{Z_2}$$

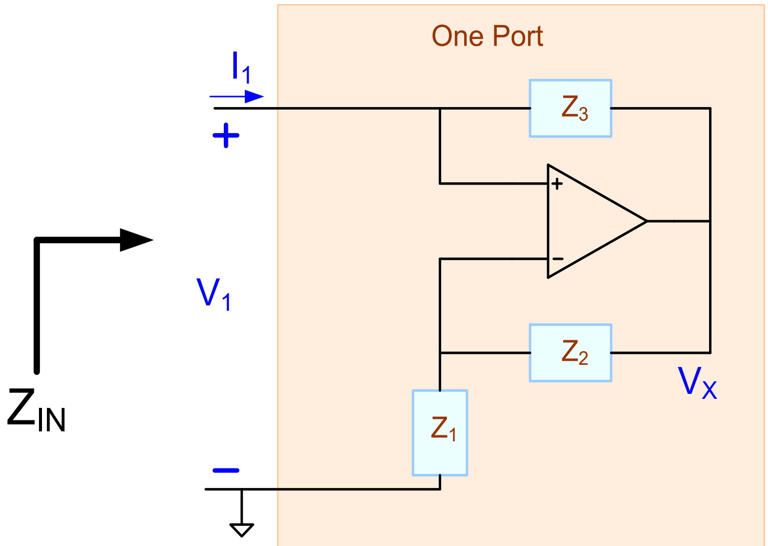
If $Z_1=R_1$, $Z_2=R_2$ and $Z_3=R_3$, $$Z_{IN} = -\frac{R_1 R_3}{R_2}$$ This is a negative resistor !

If $Z_2=1/sC$, $Z_1=R_1$ and $Z_3=R_3$, $$Z_{IN} = -sCR_1R_3$$ This is a negative inductor !

If $Z_2=R_2$, $Z_1=1/sC$ and $Z_3=R_3$, $$Z_{IN} = -\frac{R_3}{sCR_2}$$ This is a negative capacitor !

This is termed a Negative Impedance Converter

Impedance Converters



$$Z_{IN} = -\frac{Z_1 Z_3}{Z_2}$$

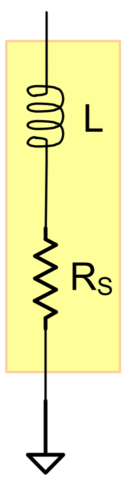
If $Z_2 = 1/sC$, $Z_1 = R_1$ and $Z_3 = R_3$, $\quad Z_{IN} = -sCR_1R_3$

Modification of NIC to provide a positive inductance:

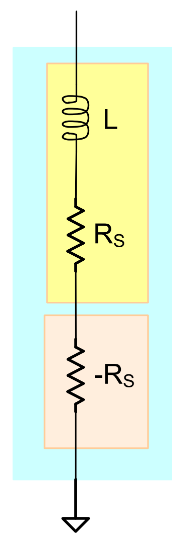
Replace Z_1 itself with a second NIC that has a negative input impedance

Negative Impedance Converter

One application of NIC



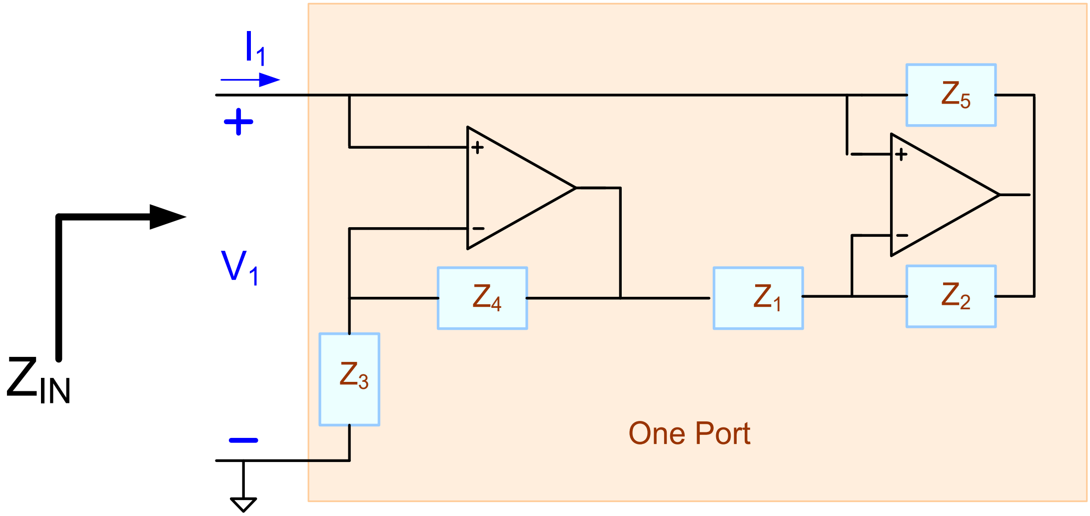
Lossy
Inductor



If select components so that $R_S = \frac{R_2}{R_1R_3}$

Lossless
Inductor

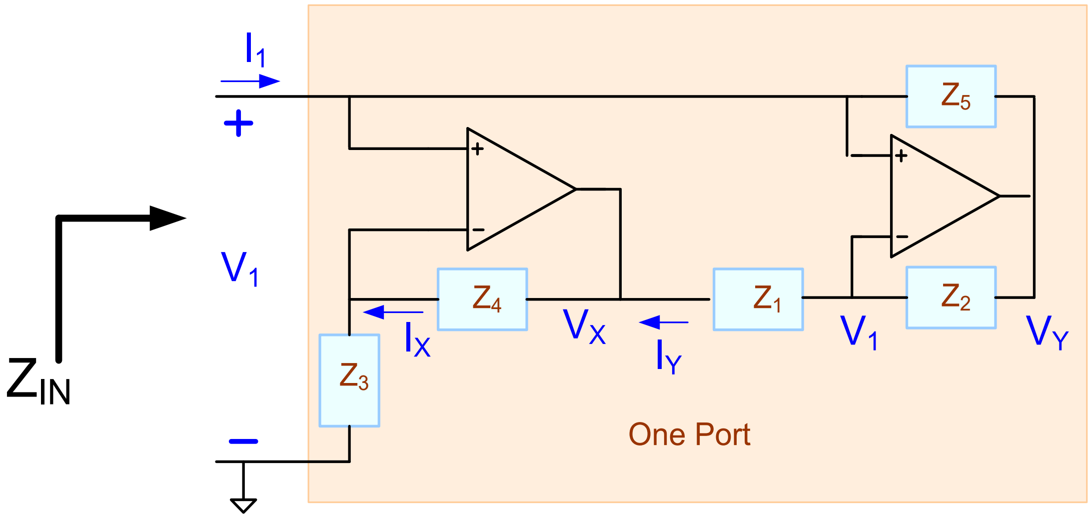
Impedance Converters



$$Z_{IN} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4}$$

This circuit is often called a Gyrator

Gyrator Analysis



$$I_X = V_1 G_3$$

$$V_X = V_1 + V_1 G_3 / G_4 \;= V_1\left(1 + \frac{G_3}{G_4}\right)$$

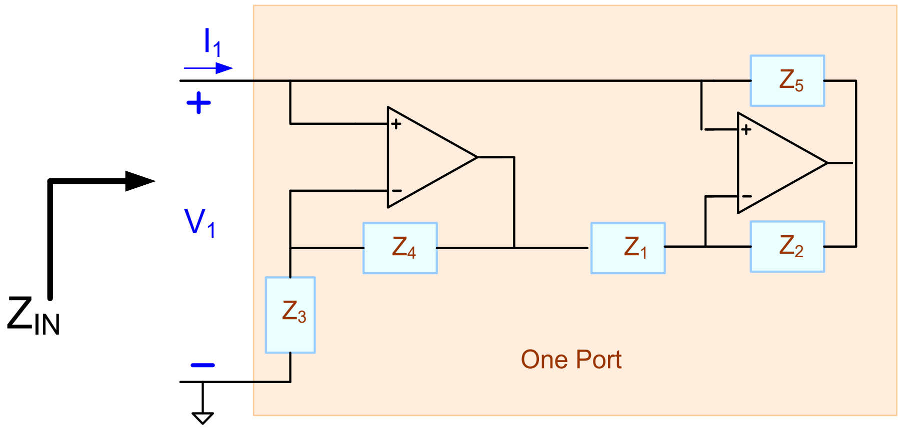
$$I_Y = (V_1 - V_X) G_1 \;= V_1\left(-\frac{G_3}{G_4}\right) G_1$$

$$V_Y = V_1 + I_Y / G_2 \;= V_1\left(1 - \frac{G_3}{G_4}\left(\frac{G_1}{G_2}\right)\right)$$

$$I_1 = (V_1 - V_Y) G_5 = V_1\left(\frac{G_3}{G_4}\left(\frac{G_1}{G_2}\right)\right) G_5$$

$$Z_{IN} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4}$$

Gyrator Applications



$$Z_{IN} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4}$$

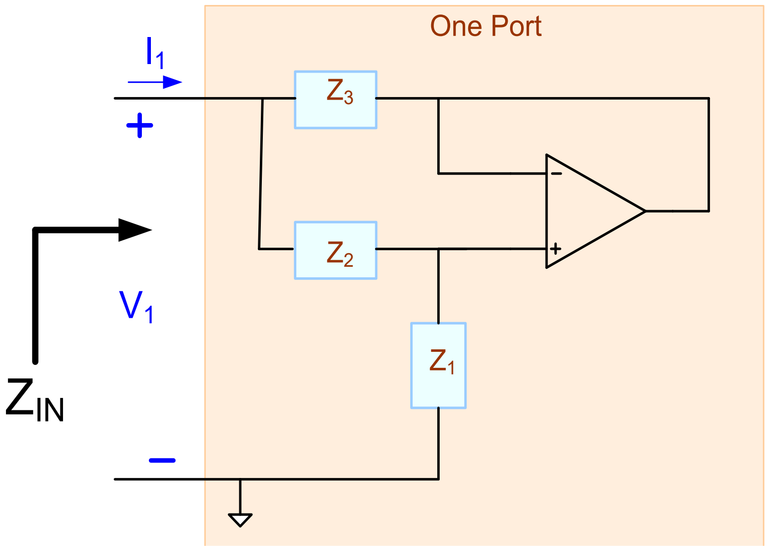
If $Z_1 = Z_3 = Z_4 = Z_5 = R$ and $Z_2 = 1/sC$ $\quad Z_{IN} = (R^2C)s \quad$ This is an inductor of value $L = R^2C$

If $Z_2 = R_2$, $Z_3 = R_3$, $Z_4 = R_4$, $Z_5 = R_5$ and $Z_1 = 1/sC$ $\quad Z_{IN} = \frac{R_3 R_5}{sCR_2R_4}$

This is a capacitor of value $\quad C_{EQ} = C\frac{R_2R_4}{R_3R_5} \quad$ (can scale capacitance up or down)

If $Z_2 = Z_4 = Z_5 = R$ and $Z_1 = Z_3 = 1/sC$ $\quad Z_{IN} = (R^3C^2)s^2 \quad$ This is a “super” capacitor of value R^3C^2

Impedance Converters

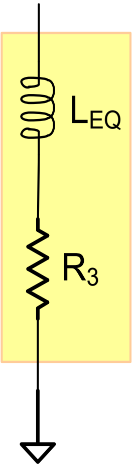


$$I_1 = \left(V_1 - \left(\frac{Z_1}{Z_1 + Z_2} \right) V_1 \right) G_3$$

$$Z_{IN} = Z_3 \left(1 + \frac{Z_2}{Z_1} \right)$$

If $Z_3 = R_3$, $Z_2 = R_2$ and $Z_1 = 1/sC$

$$Z_{IN} = R_3 + s\left(CR_2R_3 \right)$$



$$L_{EQ} = CR_2R_3$$

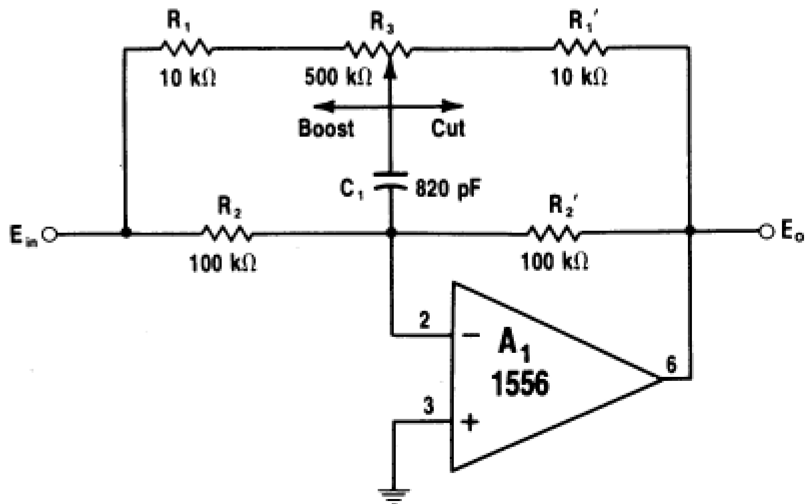
Basic Filter Components

- All Pass Networks
- Arbitrary Transfer Function Synthesis
- Impedance Transformation Circuits
- Equalizers

Shelving Equalizers

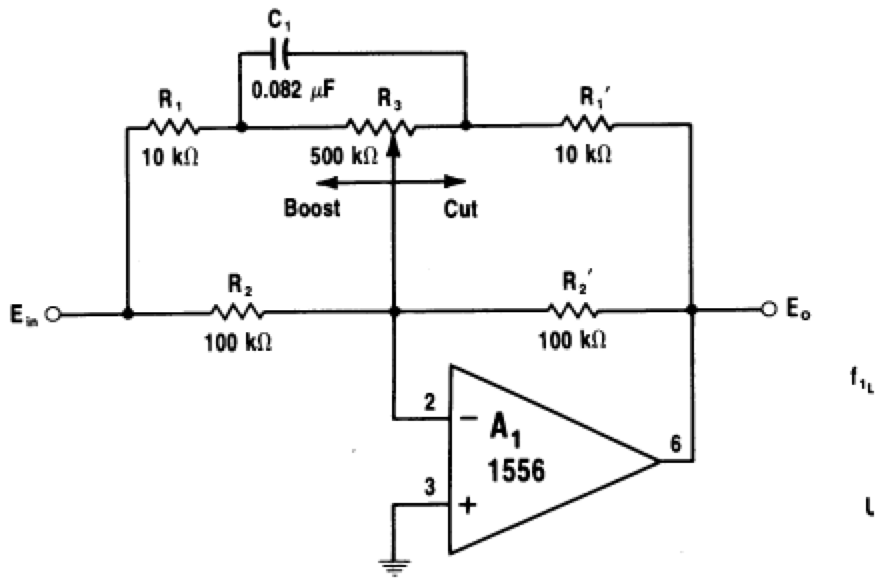
- Widely used in audio applications
- User-programmable filter response

Shelving Equalizers



(A) High frequency.

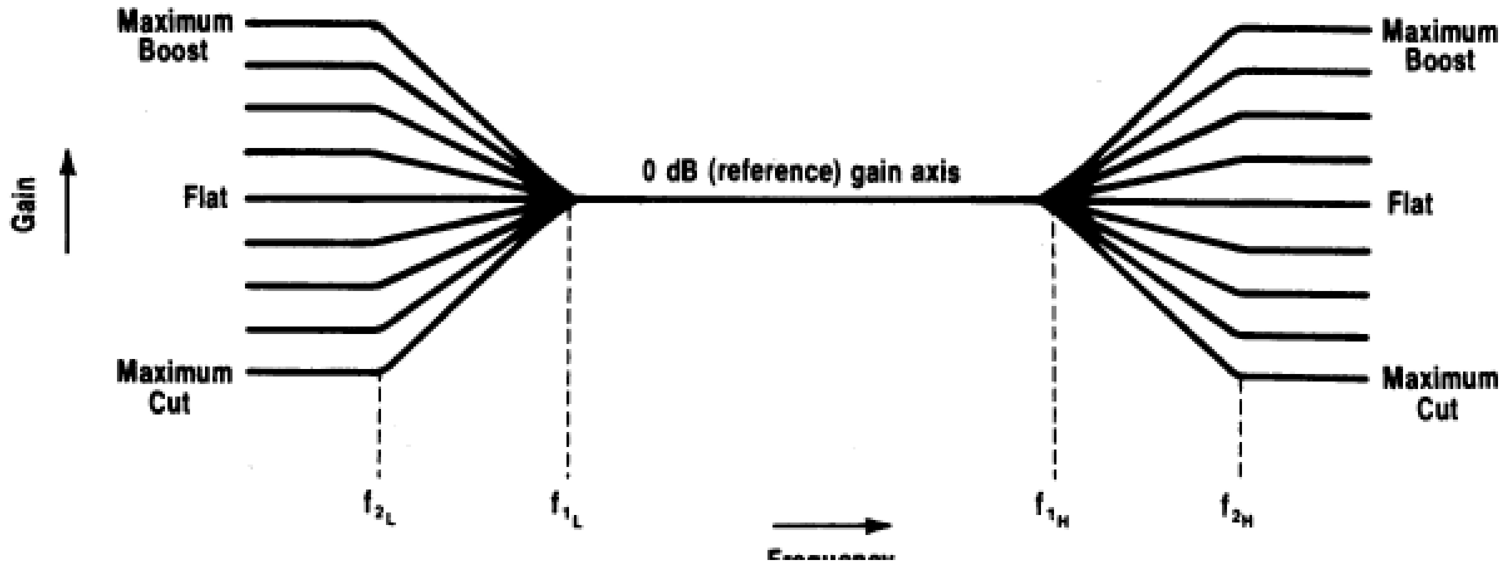
Shelving Equalizers



(B) Low frequency.

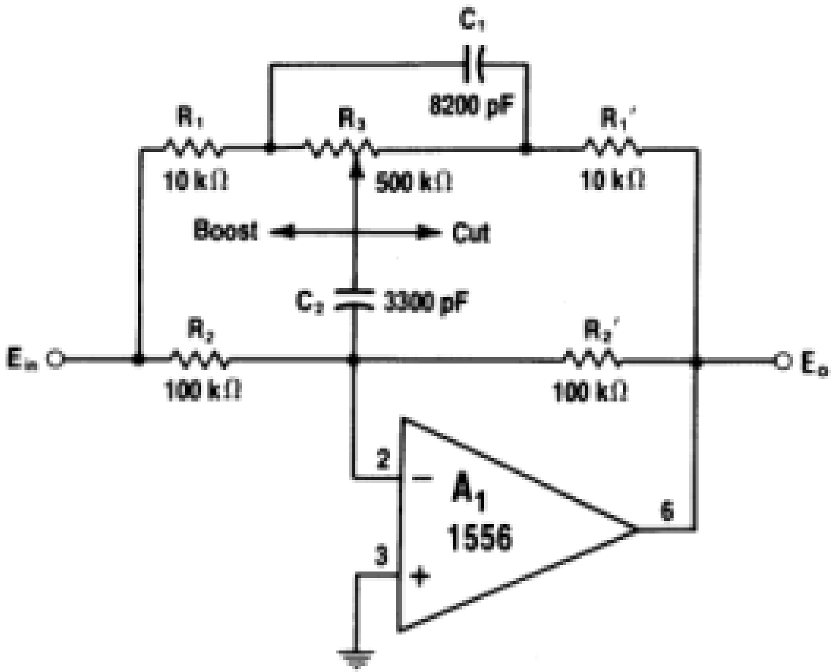
Fig. 6-37. Shelving equalizers.

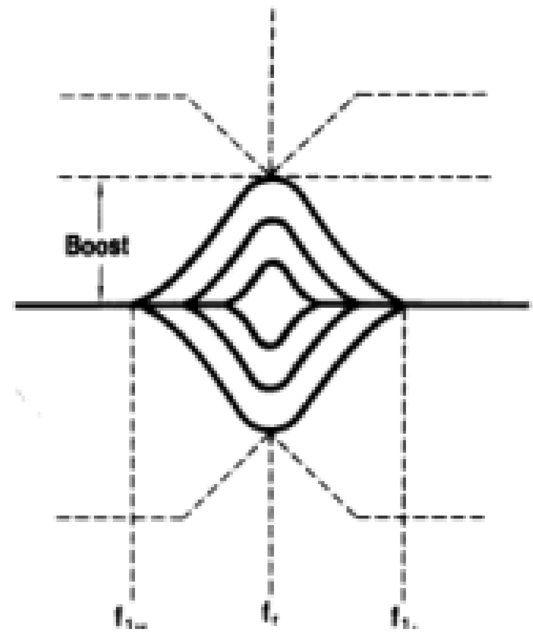
Shelving Equalizers



- The expressions for f_L and f_H for the previous two circuits show a small movement with the potentiometer position in contrast to the fixed point location depicted in this figure

- The OTA-C filters discussed earlier in the course can be designed to have fixed values for f_L and f_H when cut or boost is used.


C1
8200 pF
R1
10 kΩ
R3
500 kΩ
R1'
10 kΩ
Boost
Cut
C2
3300 pF
Ein
R2
100 kΩ
R2'
100 kΩ
Eo
2
3
A1
1556
6


Boost

Selected Recent Publications on Analog Filter Design

ISCAS 2024

0.5V 32nW Inverter-Based Gm-C Filter for Bio-Signal Processing

Ali Namdari, Orazio Aiello, Daniele D. Caviglia
[1] DITEN, University of Genova
ali.namdari@edu.unige.it; orazio.aiello@unige.it; daniele.caviglia@unige.it

180nm CMOS   w0: 470 Hz

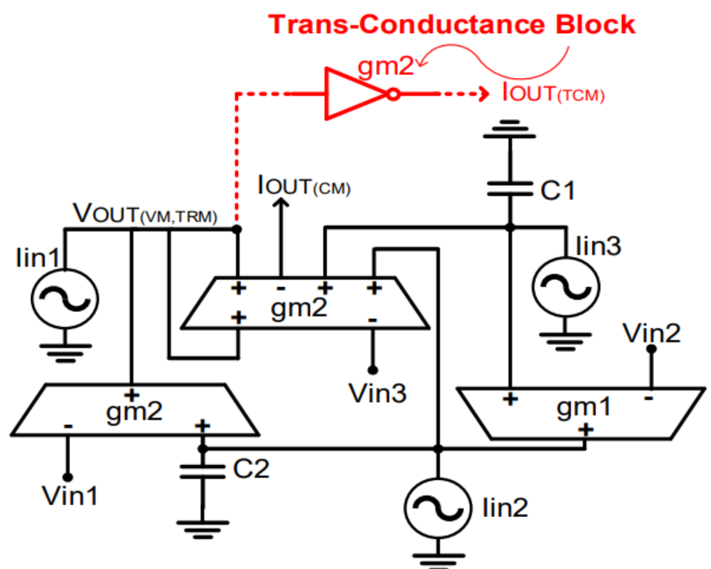


Fig.1. The proposed universal multi-mode Gm-C filter

0.5 V Fully Differential Universal Filter Based on Multiple Input OTAs

WINAI JAIKLA[1], FABIAN KHATEB[2,6], MONTREE KUMNGERN[3], TOMASZ KULEJ[4], RAJEEV KUMAR RANJAN[5], (Member, IEEE), AND PEERAWUT SUWANJAN[1]

IEEE Access, Oct 2020

180nm Process, fo=1Hz

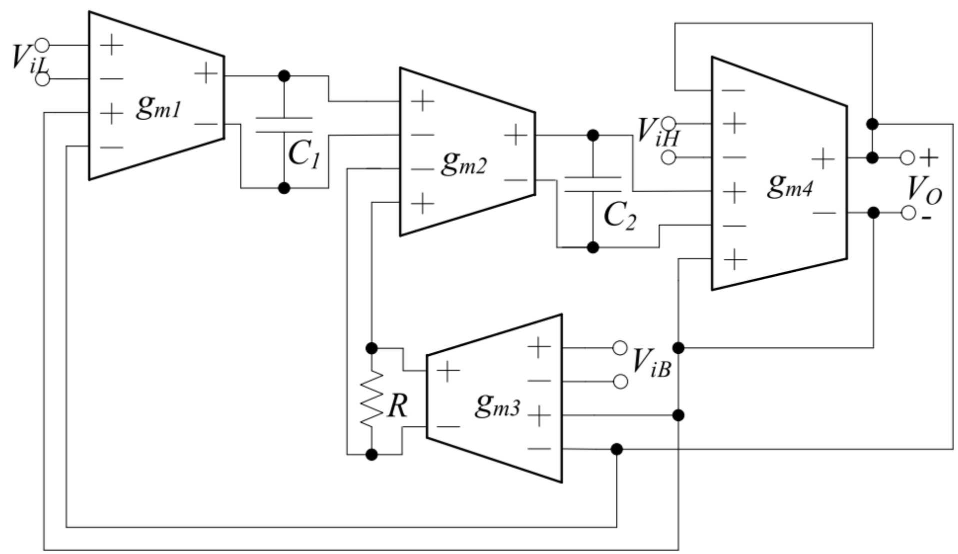


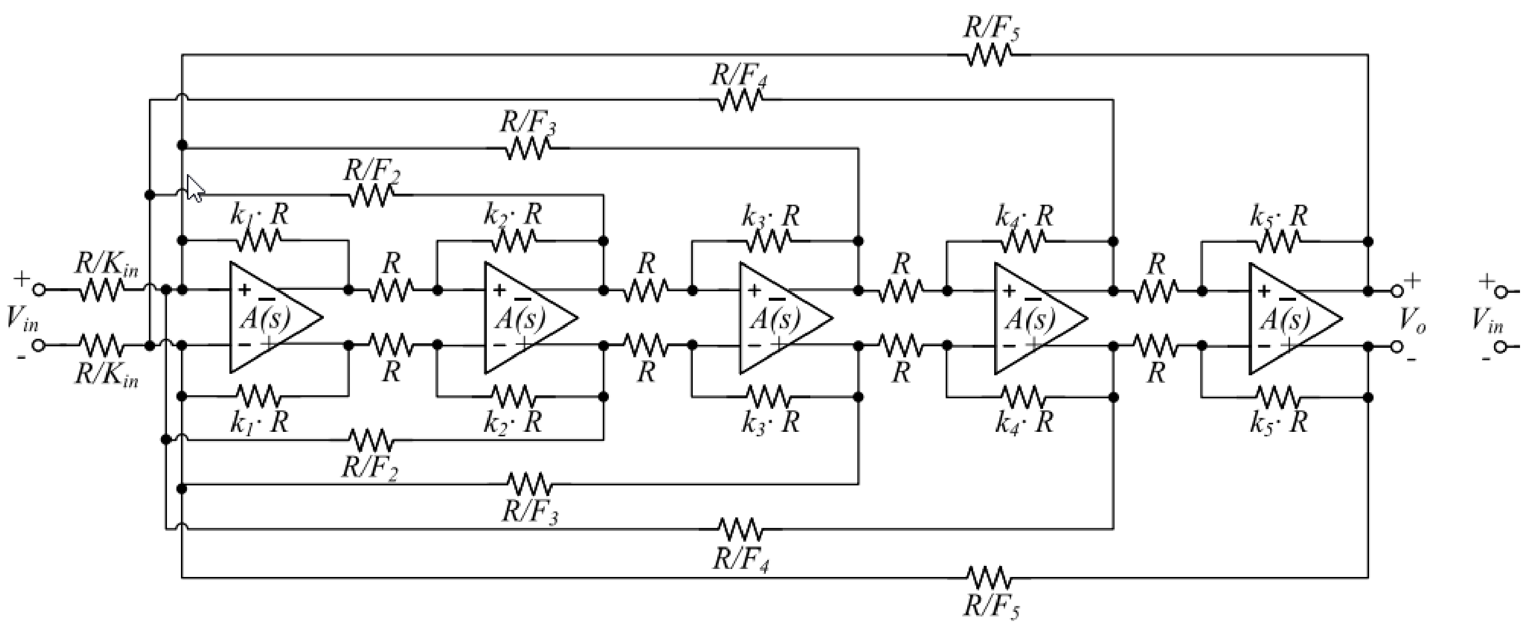
FIGURE 3. **Proposed fully differential universal filter.**

TCAS I May 2021

Synthesis of High-Order Continuously Tunable Low-Pass Active-R Filters

Adriana C. Sanabria-Borbón, *Member, IEEE*, and Edgar Sánchez-Sinencio, *Life Fellow,*

TSMC 180nm process, w_0 from 1 to 50 MHz



CMOS Analog Filter Design for Very High Frequency Applications

Luis Abraham Sánchez-Gaspariano [1,*], Carlos Muñiz-Montero [2], Jesús Manuel Muñoz-Pacheco [1], Carlos Sánchez-López [3], Luz del Carmen Gómez-Pavón [1], Arnulfo Luis-Ramos [1] and Alejandro Israel Bautista-Castillo [2]

180nm process, approx. 400MHz operation

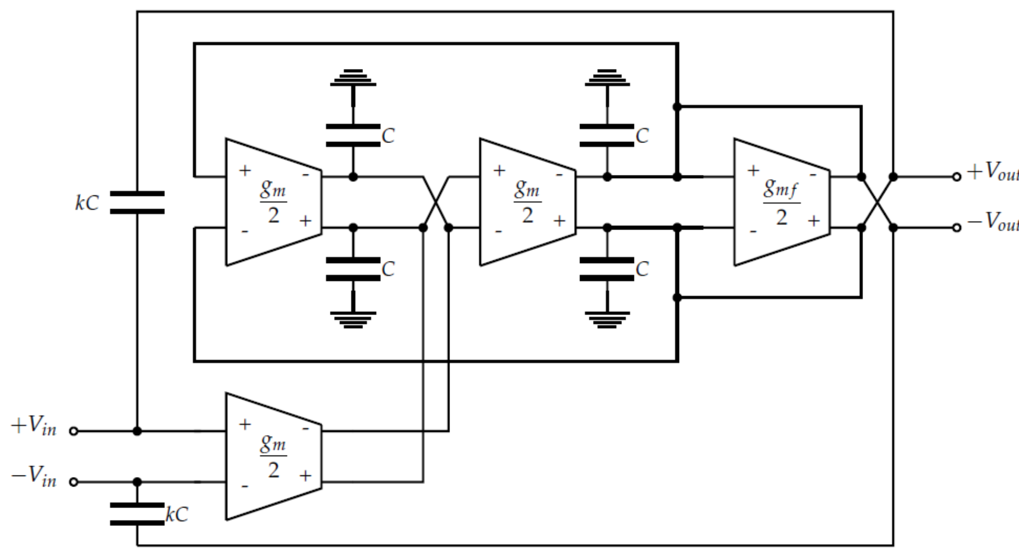


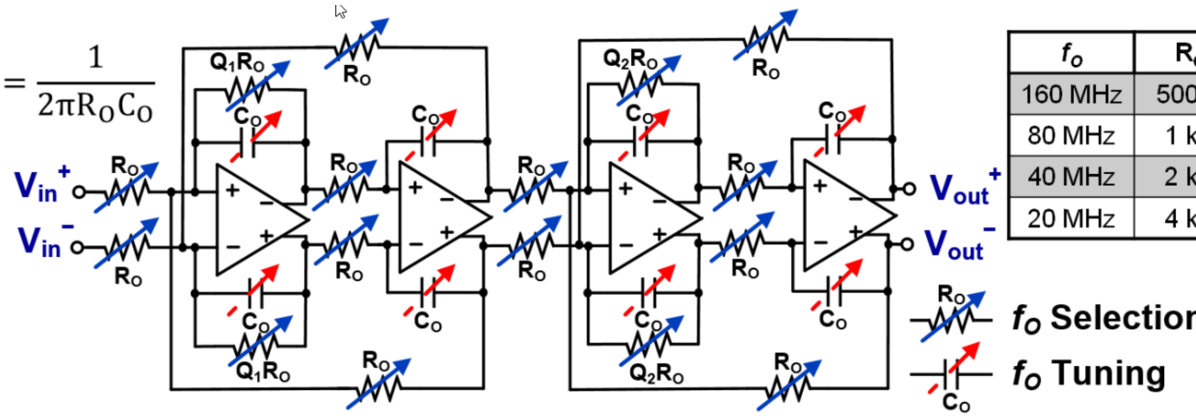
Figure 5. Q enhanced bandstop *gm-C* biquad filter.

A 0.6-V Power-Efficient Active-RC Analog Low-Pass Filter With Cutoff Frequency Selection

Fernando Lavalle-Aviles, *Member, IEEE*, and Edgar Sánchez-Sinencio, *Life Fellow, IEEE*

130 nm CMOS Process

$$f_O = \frac{1}{2\pi R_O C_O}$$



f_O	R_O	C_O
160 MHz	500 Ω	2 pF
80 MHz	1 kΩ	2 pF
40 MHz	2 kΩ	2 pF
20 MHz	4 kΩ	2 pF

Fig. 1. FD LV fourth-order Butterworth filter implementation.

JSC July 2020

Analysis and Design of a 260-MHz RF Bandwidth +22-dBm OOB-IIP3 Mixer-First Receiver With Third-Order Current-Mode Filtering TIA

Giacomo Pini, *Student Member, IEEE*, Danilo Manstretta, *Member, IEEE*, and Rinaldo Castello, *Life Fellow, IEEE*

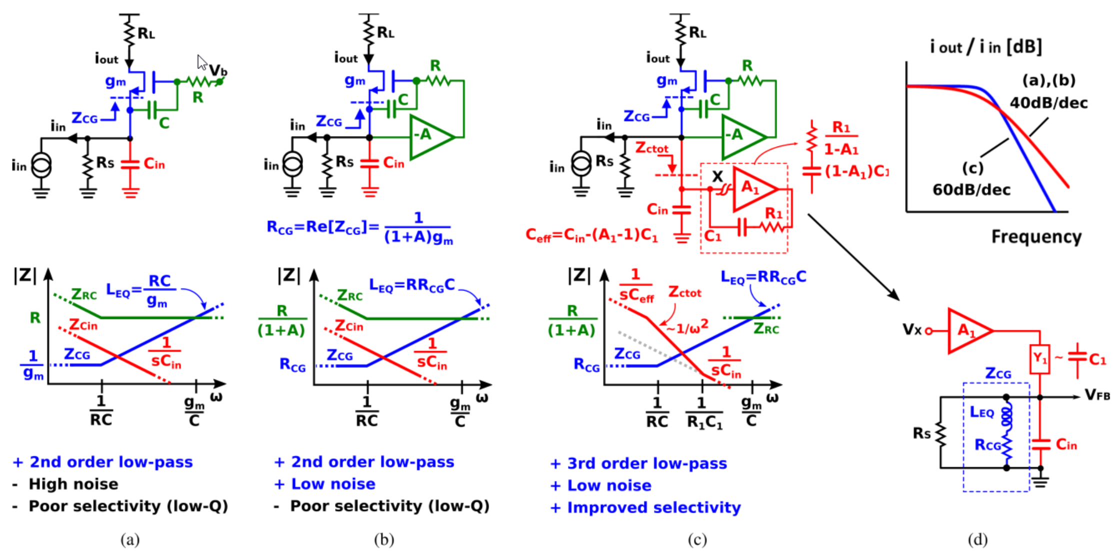


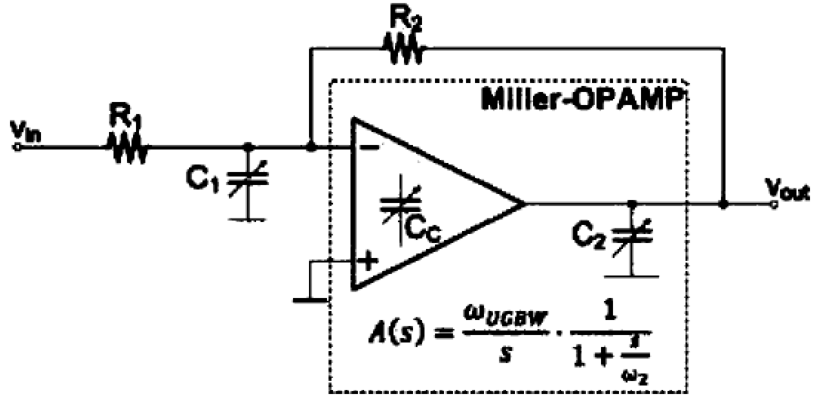
Fig. 1. Schematic representation of the CG-based TIAs and the corresponding impedance magnitude plots. (a) Filtering CG, (b) regulated cascode, (c) regulated cascode with frequency-dependent negative capacitance, and (d) simplified schematic for loop gain calculation and i_{out}/i_{in} frequency response of (a)–(c).

A 0.9V 3rd-Order Single-OPAMP Analog Filter in 28nm CMOS-bulk

Marcello De Matteis[1,2], Andrea Donno[3,4], Stefano Marinaci[4], Stefano D'Amico[3,4], Andrea Baschirotto[1,2]

From IEEE Int. Workshop on Advances in Sensors and Interfaces, June 2017

"The scheme take advantage of the efficient Active-gm-RC filter [3], which exploits the Opamp unity gain bandwidth (COUGBW) to synthesize the transfer function."



g. 1 – Single ended architecture of the proposed analog filter

Tab. I – Targeted filter transfer function parameters

Parameter	This Design
ω_{23} – real pole frequency	$2\cdot\pi\cdot350$MHz
ω_0 – complex poles frequency	$2\cdot\pi\cdot160$MHz
Q_0 – complex pole quality factor	0.9
f_{-3dB}- cut-off frequency	$2\cdot\pi\cdot132$MHz
G – low pass filter dc-gain	0dB

[3] A. Donno, S. D'Amico, M. De Matteis, A. Baschirotto "A 150MHz 3rd-order single Opamp continuous-time analog filter in 28nm CMOS technology" Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2015, Cairo (Egypt); 6-9 December 2015 (DOI: 10.1109/ICECS.2015.7440274).

A 0.9V 600MHz 4th-Order Analog Filter with Feed-Forward Compensated OPAMP in CMOS 28nm F. Ciciotti, M. De Matteis, and A. Baschirotto

PRIME Conference, June 2017

“The transfer function is obtained with the cascade of two Active-RC Rauch biquadratic cells. Each cell is based on a novel OPAMP optimized for very high frequency operation achieving a Unity Gain Bandwidth (UGBW) > 7GHz.”

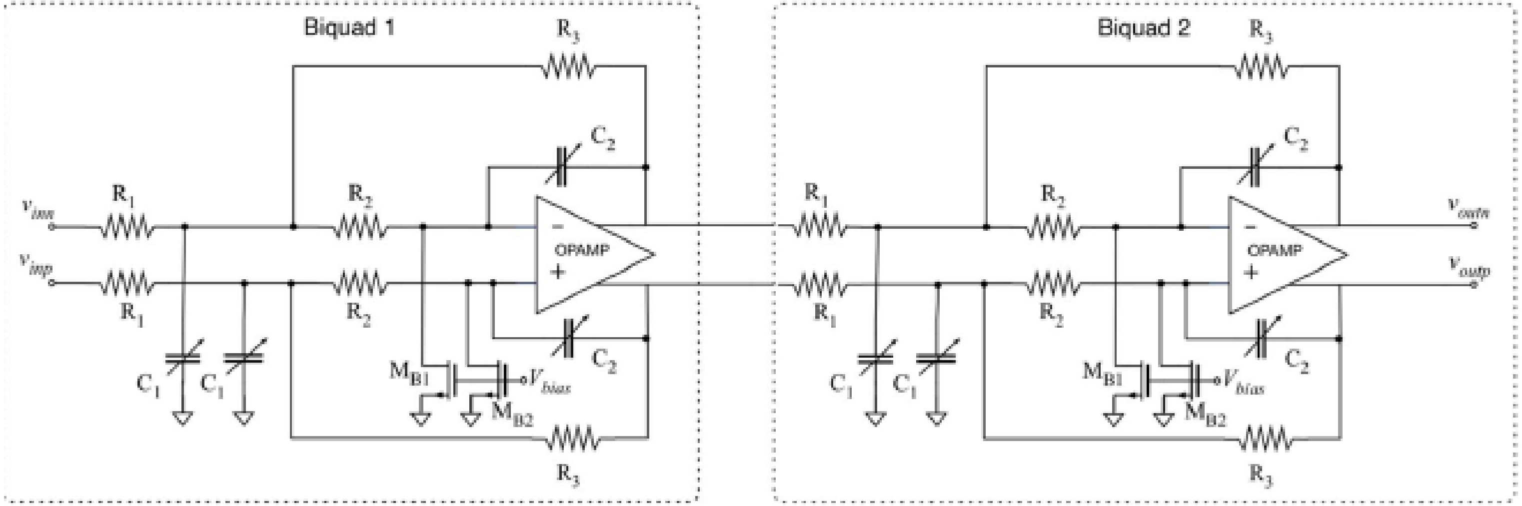
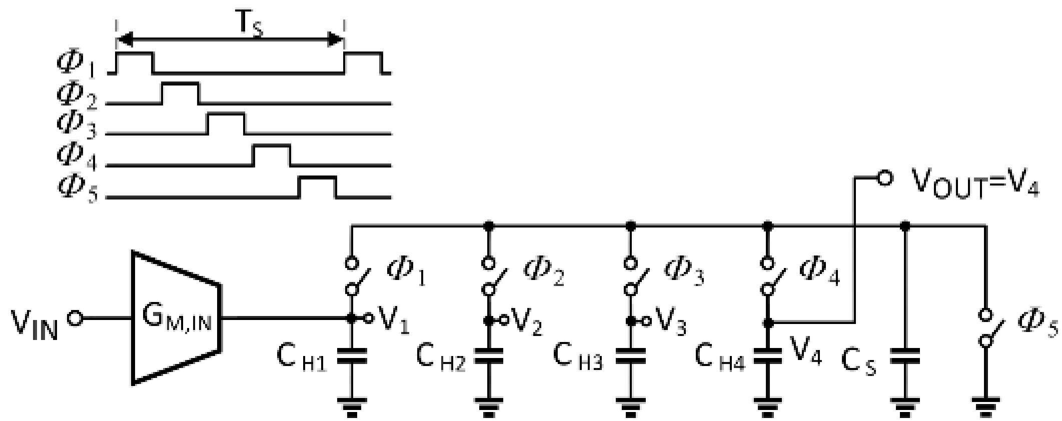


Fig. 1. Filter chain.

This is actually a bridged-T structure !

SC Filter w/o Op Amp

M. Tohidian, I. Madadi, and R. B. Staszewski, "Analysis and design of a high-order discrete-time passive IIR low-pass filter," *IEEE J. Solid-State Circuits*, vl. 49, no. 11, pp. 2575–2587, Nov. 2014.



. 1. A 4^{th}-order real-pole passive-SC LPF [2].

SC Filter w/o Op Amp

S. Iida, “Filter circuit, integrated circuit, communication module, and communication apparatus,” U.S. Patent 0 334 348 A1, Nov. 13, 2014.

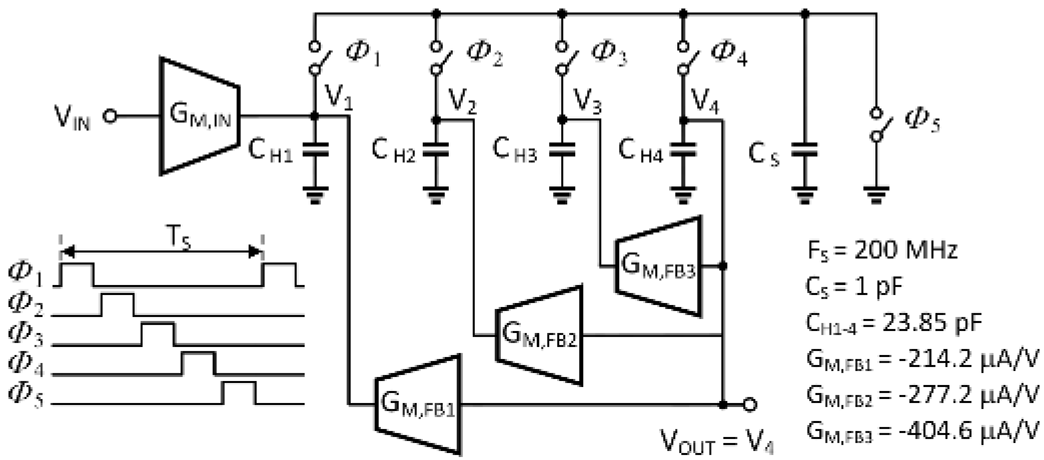


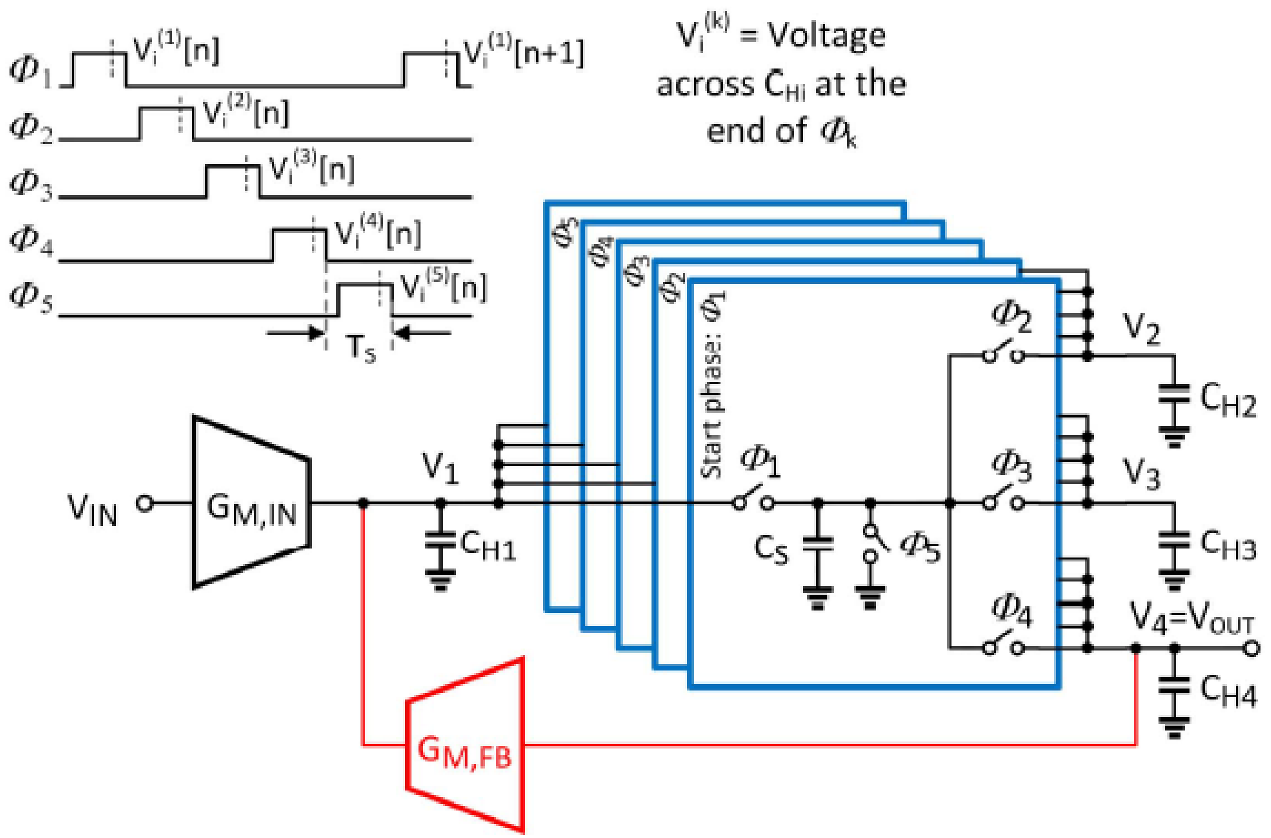
Fig. 3. A 4^{th}-order complex-pole filter [21].

SC Filter w/o Op Amp

A 0.49–13.3 MHz Tunable Fourth-Order LPF with Complex Poles Achieving 28.7 dBm OIP3

Pedram Payandehnia, *Student Member, IEEE*, Hamidreza Maghami, *Student Member, IEEE*, Hossein Mirzaie, *Student Member, IEEE*, Manjunath Kareppagoudr, *Student Member, IEEE*, Siladitya Dey, *Student Member, IEEE*, Massoud Tohidian, *Member, IEEE*, and Gabor C. Temes, *Life Fellow, IEEE*

IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS–I: REGULAR PAPERS, VOL. 65, NO. 8, AUGUST 2018

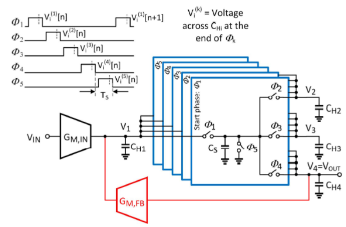


SC Filter w/o Op Amp

A 0.49–13.3 MHz Tunable Fourth-Order LPF with Complex Poles Achieving 28.7 dBm OIP3

Pedram Payandehnia, *Student Member, IEEE*, Hamidreza Maghami, *Student Member, IEEE*, Hossein Mirzaie, *Student Member, IEEE*, Manjunath Kareppagoudr, *Student Member, IEEE*, Siladitya Dey, *Student Member, IEEE*, Massoud Tohidian, *Member, IEEE*, and Gabor C. Temes, *Life Fellow, IEEE*

IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS–I: REGULAR PAPERS, VOL. 65, NO. 8, AUGUST 2018



Technology	180 nm
Order	4^{th}
VDD (V)	1.8
Power (mW)	4.3
3-dB BW (MHz)	0.49-13.3

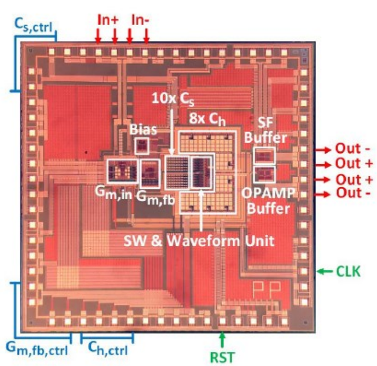
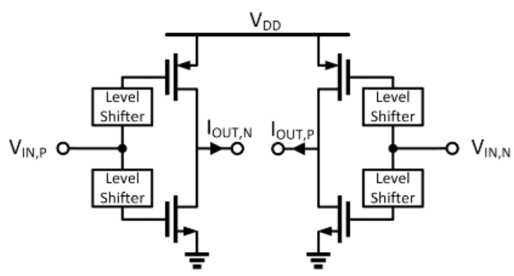
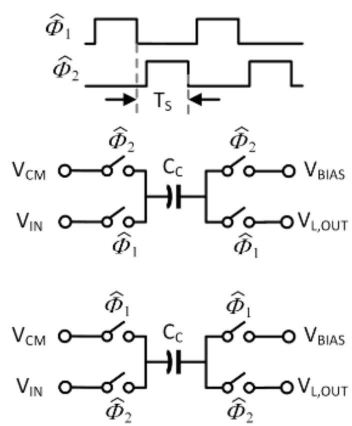


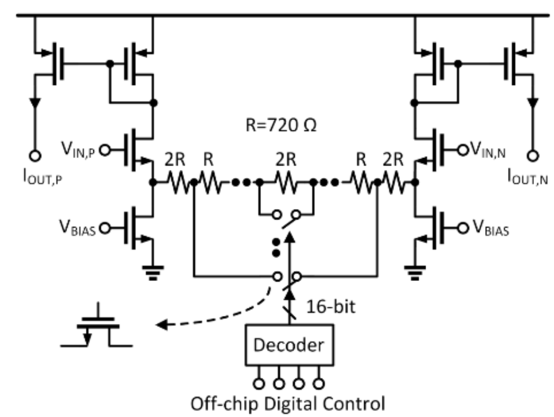
Fig. 17. Chip micrograph of the proposed filter implemented in 1P4M 180 nm CMOS technology. Die size is 4 × 4 mm.



(a)



Input OTA



Feedback OTA

A 20kHz~16MHz Programmable-Bandwidth 4th Order Active Filter using Gain-boosted Opamp with Negative Resistance in 65 nm CMOS

Jiye Lim, *Student Member, IEEE,* and Jintae Kim, *Senior Member, IEEE*

Accepted for TCAS II and pending publication Nov18

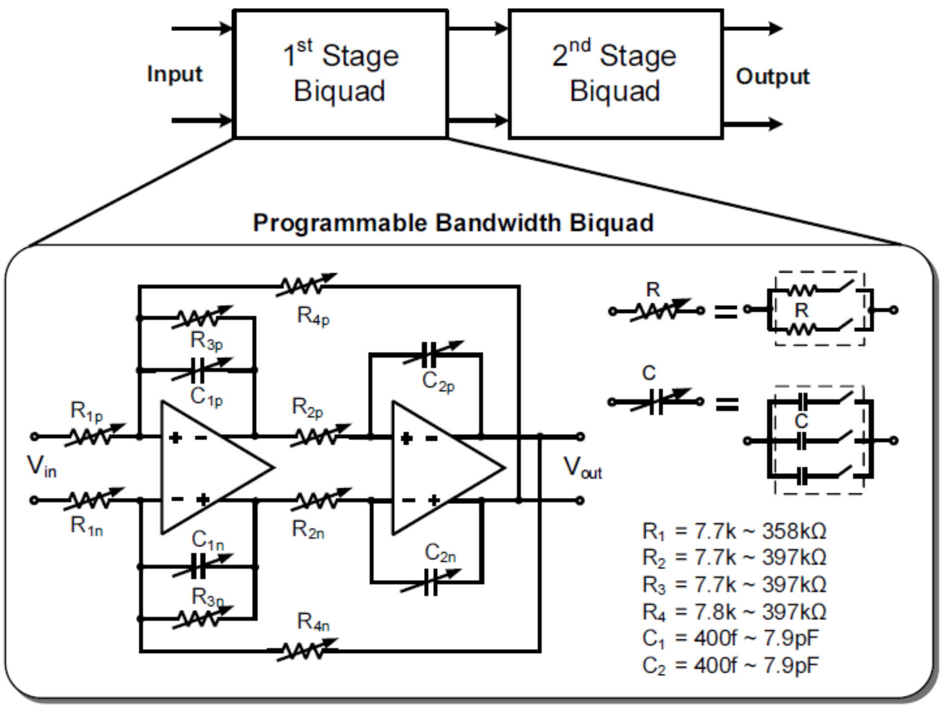


Fig. 1. A block diagram of 4th order programmable biquad filter.

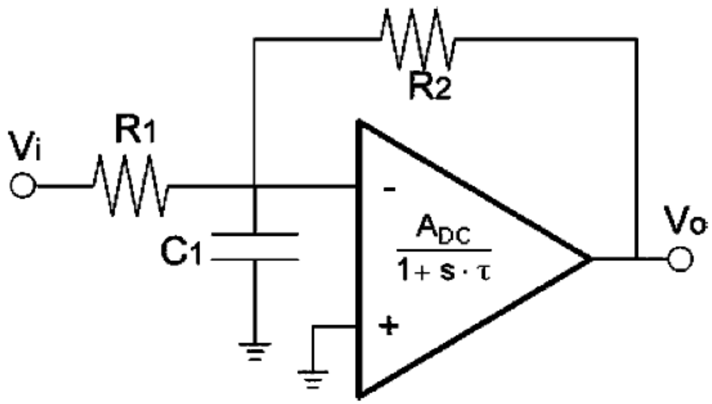
The prototype filter is fabricated in 65nm CMOS and occupies 0.098mm^2. It features three programmable cutoff frequencies of 20kHz, 2MHz, and 16MHz

Power (mW)	**19**

A 4th-Order Active-Gm-*RC* Reconfigurable (UMTS/WLAN) Filter

Stefano D'Amico, Vito Giannini, and Andrea Baschirotto

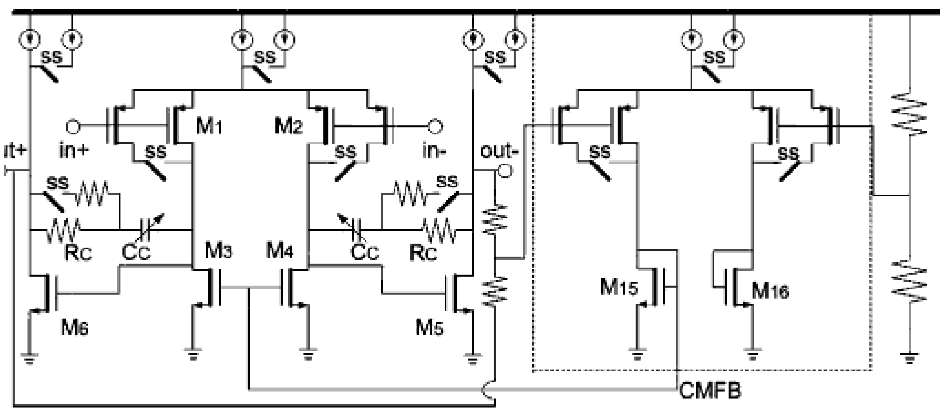
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. 7, JULY 2006



$$\left.\begin{aligned} V_{IN}G_1 + V_{OUT}G_2 &= V_X\left(G_1 + G_2 + sC\right) \\ V_{OUT} &= V_X \frac{-A_0}{1+\tau s} \end{aligned}\right\}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{-\frac{A_0 G_1}{\tau C}}{s^2 + s\left[\frac{G_1+G_2}{C} + \frac{1}{\tau}\right] + \frac{G_1 + G_2\left(1+A_0\right)}{\tau C}}$$

Active-G_m-*RC* biquadratic cell.



Differential Amp

Realizes 4th-order filter

C1 and CC tunable,
R1 and R2 switchable

Operates in 2MHz and 20MHz ranges

A 28.8-MHz 23-dBm-IIP3 3.2-mW Sallen-Key Fourth-Order Filter With Out-of-Band Zeros Cancellation Marcello De Matteis, Federica Resta, Alessandra Pipino, Stefano D'Amico, and Andrea Baschirotto

TCAS II Dec 16

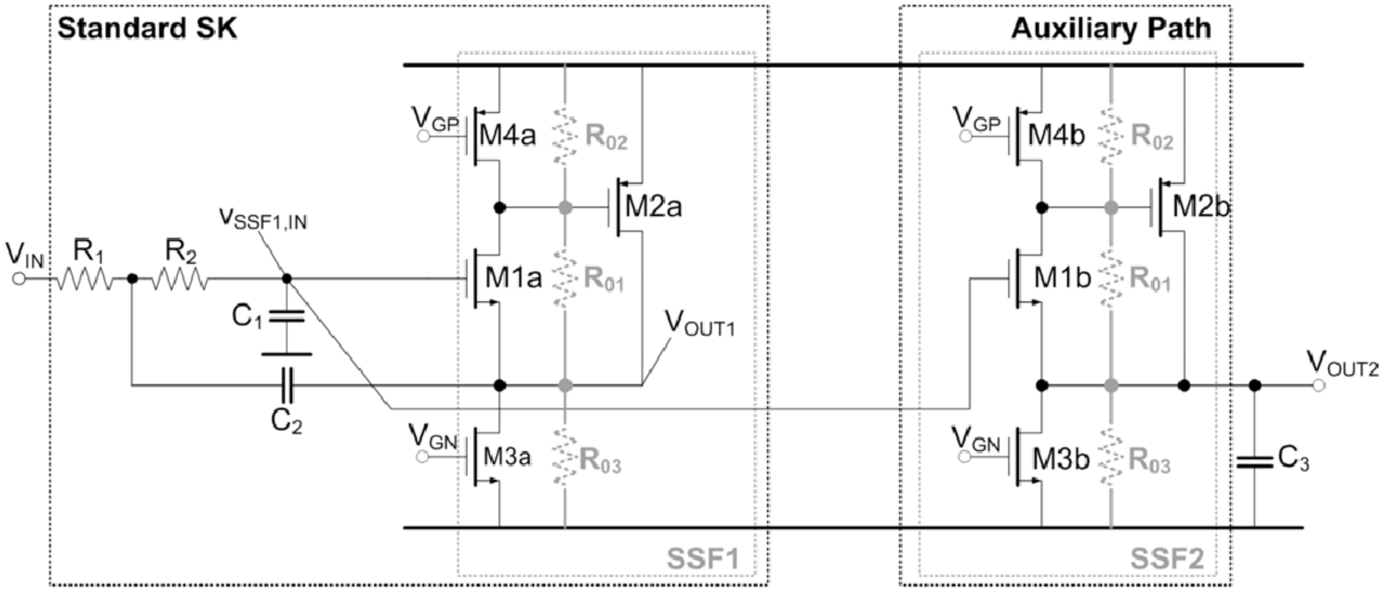


Fig. 1. SK single-ended generic scheme, with auxiliary path.

The total area occupancy is 0.12 mm^2

3.2-mW power consumption

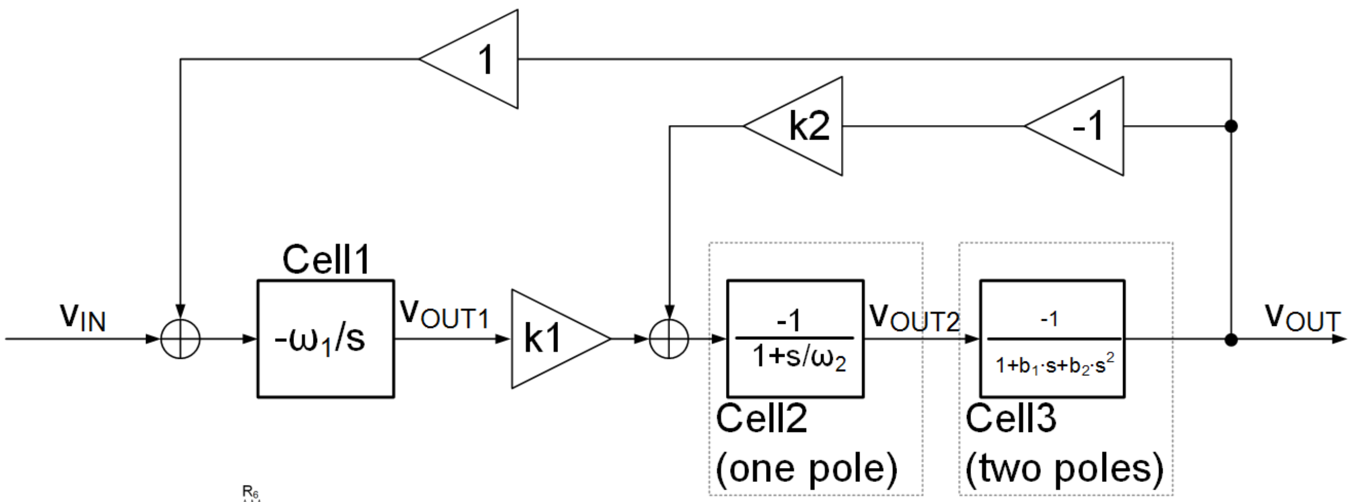
0.18u process

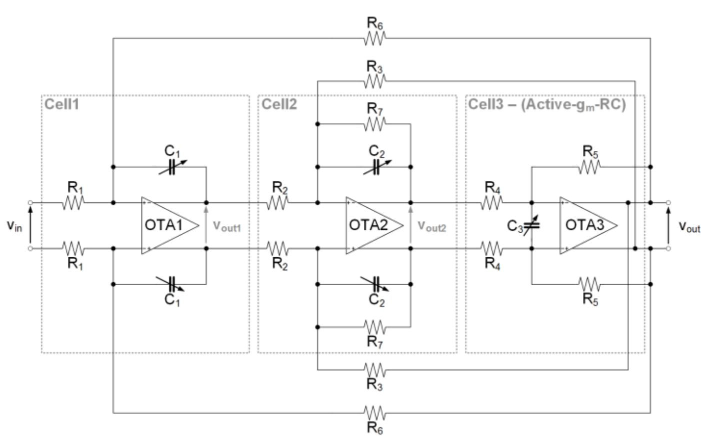
A 63-dB DR 22.5-MHz 21.5-dBm IIP3 Fourth-Order FLFB Analog Filter

Marcello De Matteis, Alessandra Pipino, Federica Resta, Alessandro Pezzotta, Stefano D’Amico, and Andrea Baschirotto

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 52, NO. 7, JULY 2017

Follow the Leader Feedback (a slight variant on the MLF approach)



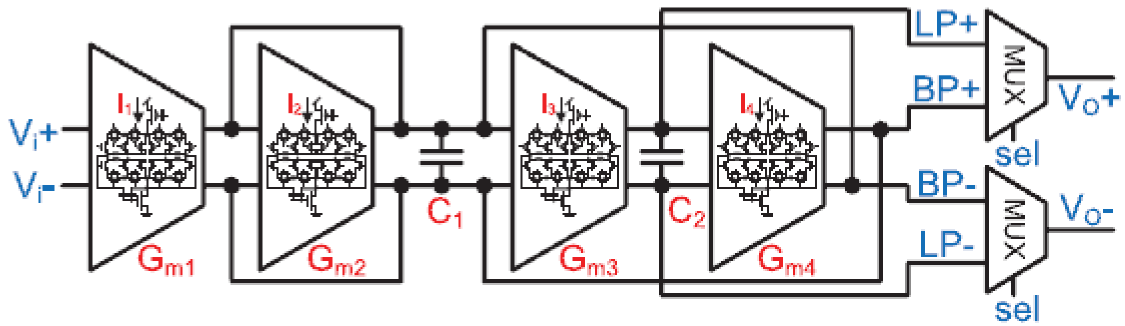


Cell 3 Realized with Gm-RC stage of previous slide

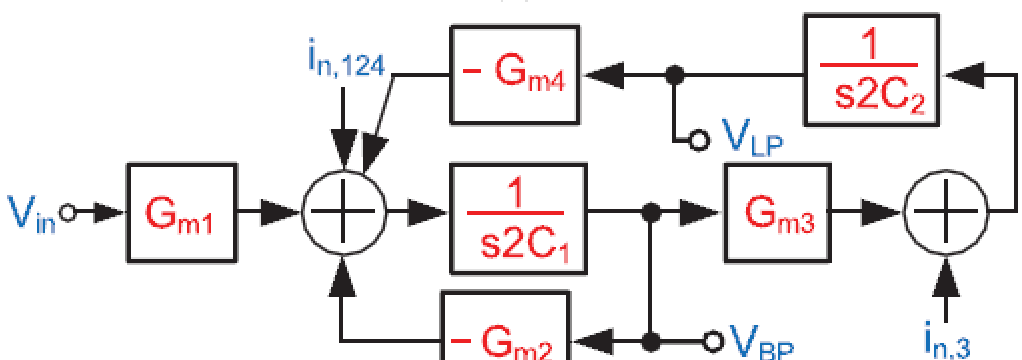
A Power-Efficient Reconfigurable OTA-C Filter for Low-Frequency Biomedical Applications

Sheng-Yu Peng, *Member, IEEE*, Yu-Hsien Lee, Tzu-Yun Wang, *Student Member, IEEE*, Hui-Chun Huang, Min-Rui Lai, Chiang-Hsi Lee, and Li-Han Liu

IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS–I: REGULAR PAPERS, VOL. 65, NO. 2, FEBRUARY 2018

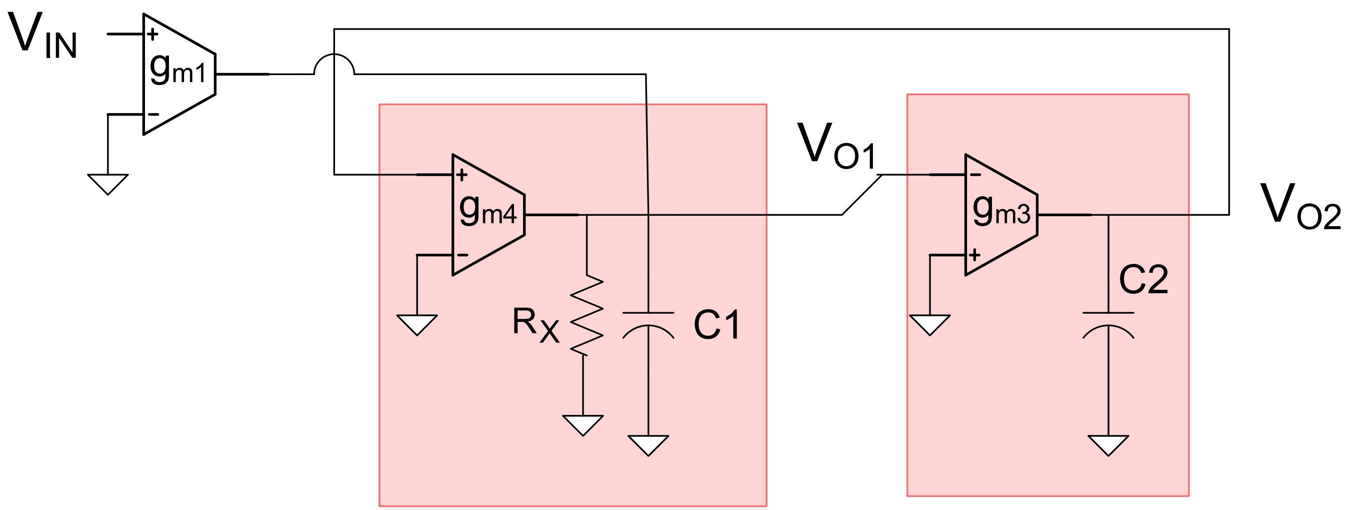


(a)



(b)

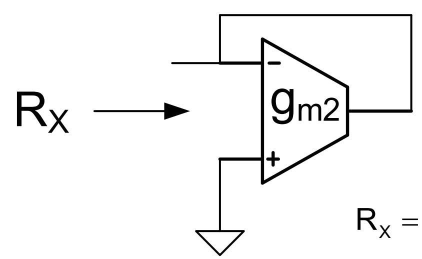
Recall the basic two-integrator loop



$$\left.\begin{aligned} V_{01}sC_1 &= G_X V_{01} + g_{m1}V_{IN} + g_{m4}V_{02} \\ V_{02}sC_2 &= g_{m3}V_{01} \end{aligned}\right\}$$

$$\frac{V_{01}}{V_{IN}} = \frac{s\dfrac{g_{m1}}{C_1}}{s^2 + s\dfrac{g_X}{C_1} + \dfrac{g_{m3}g_{m4}}{C_1C_2}}$$

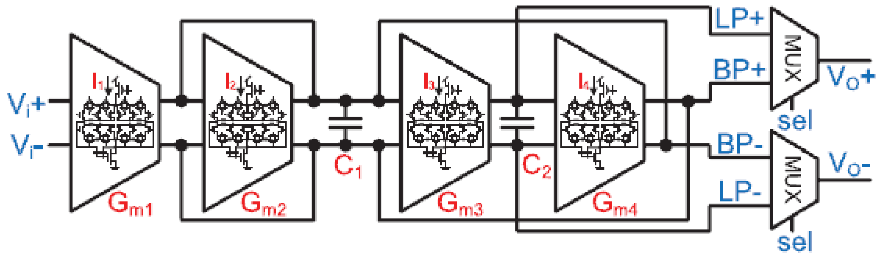
$$\frac{V_{02}}{V_{IN}} = \frac{\dfrac{g_{m3}g_{m1}}{C_1C_2}}{s^2 + s\dfrac{g_X}{C_1} + \dfrac{g_{m3}g_{m4}}{C_1C_2}}$$



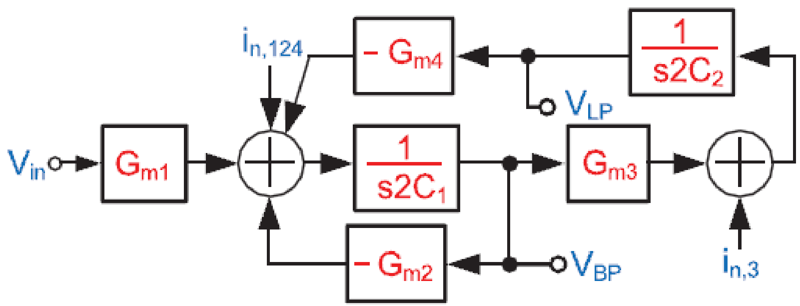
$$R_X = \frac{1}{g_{m2}}$$

$$\frac{V_{01}}{V_{IN}} = \frac{s\dfrac{g_{m1}}{C_1}}{s^2 + s\dfrac{g_{m2}}{C_1} + \dfrac{g_{m3}g_{m4}}{C_1C_2}}$$

$$\frac{V_{02}}{V_{IN}} = \frac{\dfrac{g_{m3}g_{m1}}{C_1C_2}}{s^2 + s\dfrac{g_{m2}}{C_1} + \dfrac{g_{m3}g_{m4}}{C_1C_2}}$$



(a)

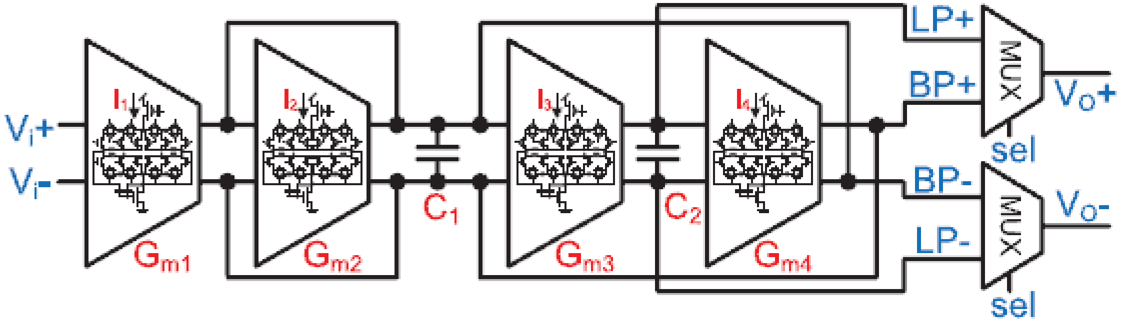


(b)

- This is a fully-differential implementation of the standard two-integrator loop
- MUX selects either LP or BP output

$$\frac{V_{01}}{V_{IN}} = \frac{s\frac{g_{m1}}{C_1}}{s^2 + s\frac{g_{m2}}{C_1} + \frac{g_{m3}g_{m4}}{C_1C_2}}$$

$$\frac{V_{02}}{V_{IN}} = \frac{\frac{g_{m3}g_{m1}}{C_1C_2}}{s^2 + s\frac{g_{m2}}{C_1} + \frac{g_{m3}g_{m4}}{C_1C_2}}$$



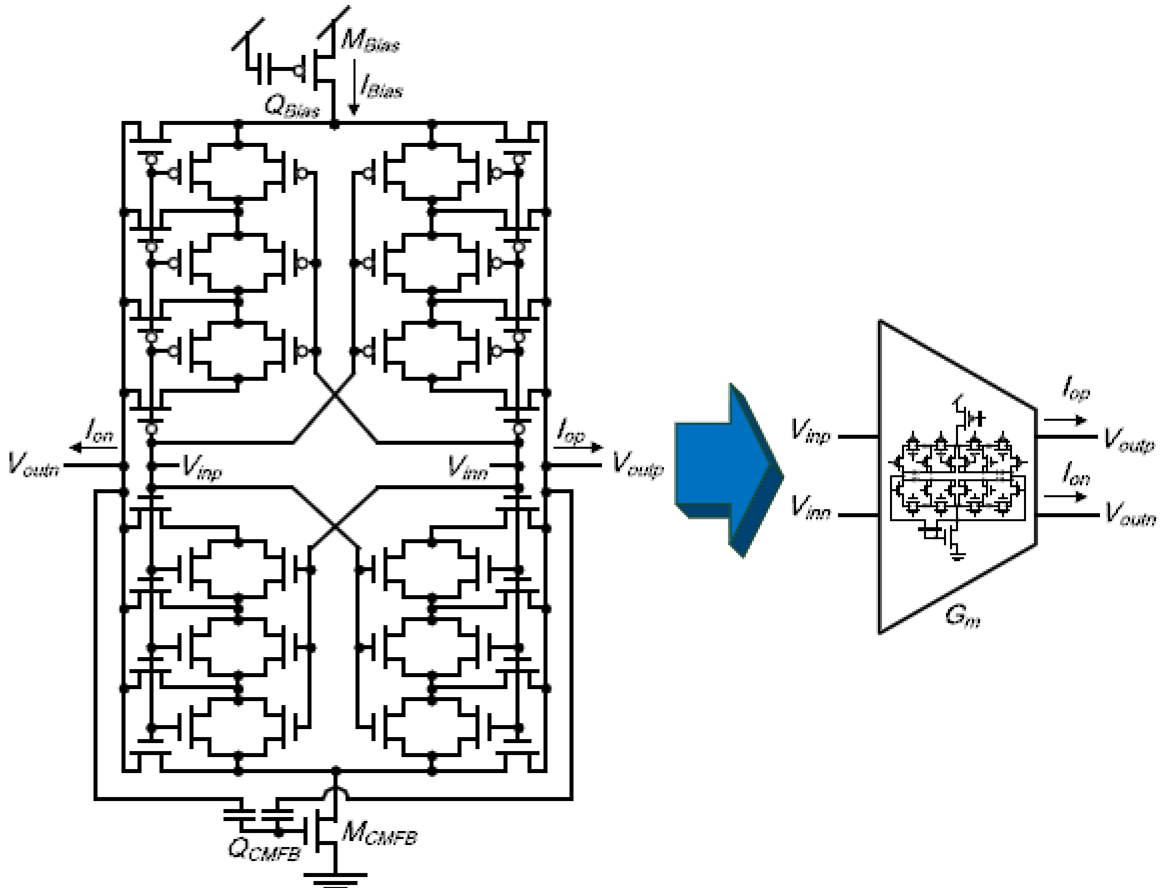
- This is a fully-differential implementation of the standard two-integrator loop
- MUX selects either LP or BP output

$$\frac{V_{01}}{V_{IN}} = \frac{s\frac{g_{m1}}{C_1}}{s^2 + s\frac{g_{m2}}{C_1} + \frac{g_{m3}g_{m4}}{C_1C_2}}$$

$$\frac{V_{02}}{V_{IN}} = \frac{\frac{g_{m3}g_{m1}}{C_1C_2}}{s^2 + s\frac{g_{m2}}{C_1} + \frac{g_{m3}g_{m4}}{C_1C_2}}$$

OTAs operate in weak inversion
Adjust ω0 by changing tail currents – claim in excess of 5 decades of adjustment
Target 2Hz to 20KHz though claim can go much lower (claim to 10mHz range) and higher
Bias current adjusted by changing charge on floating gate transistor
Each biquad requires 0.12mm^2 of die area in 350nm process

Linearized OTA

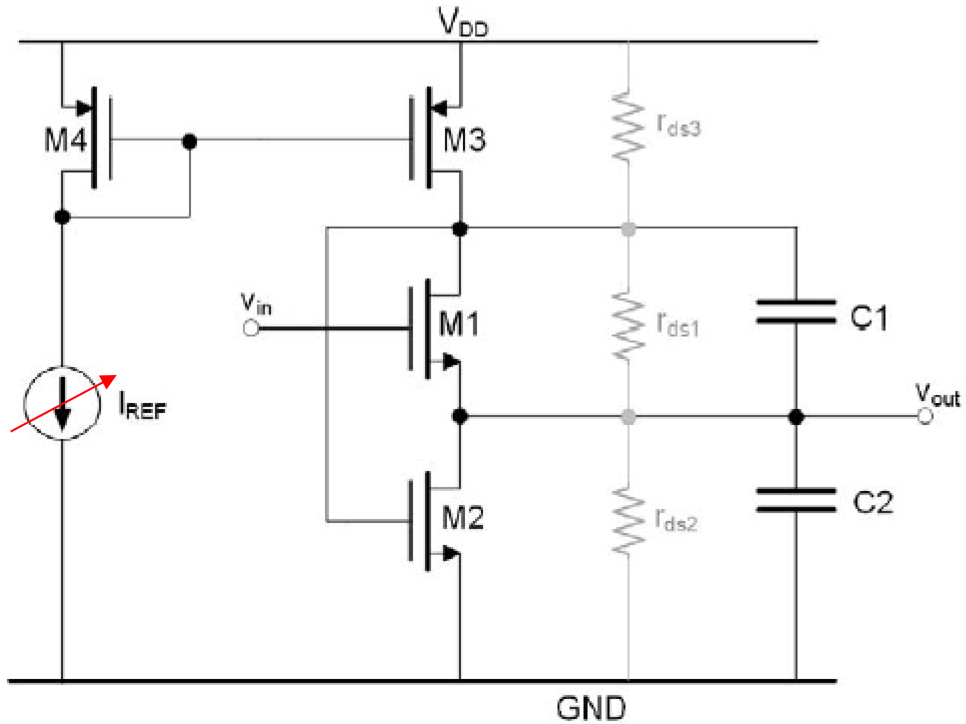


Used computer iteration to size devices in OTA
Good linearity and low power dissipation claimed

A 28nm-CMOS 100MHz 1mW 12dBm-IIP3 4th-order Flipped-Source-Follower Analog Filter

F. Fary1, M. De Matteis1, T. Vergine1,2 and A. Baschirotto1

ESSCIRC 2018

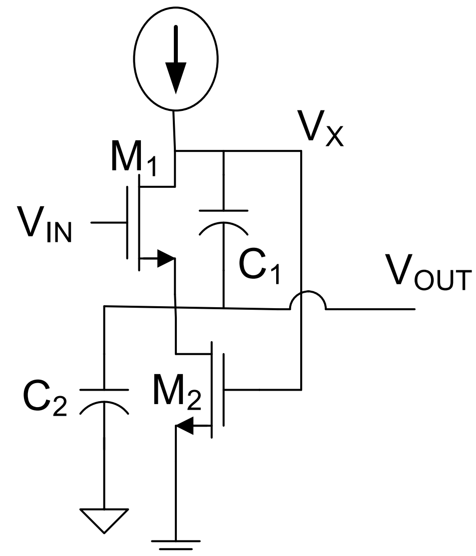


Flipped-Source-Follower NMOS Biquadratic Cell

Table 1 – Filter Design Paramters

Transfer Function		*4th-Order Low-Pass*	
dc-Gain		0dB	
Poles Frequency		100 MHz	
Cell A Q Factor	1.306	**Cell B Q Factor**	0.5412
Cell A g_{m1}- g_{m2}	1.8 mA/V	**Cell B g_{m1}- g_{m3}**	1.8 mA/V
Cell A - C_{1a}	4.8 pF	**Cell B - C_{1b}**	1.99 pF
Cell A - C_{2a}	1.75 pF	**Cell B - C_{2b}**	3.98 pF

A=0.026mm^2 for 4th order BW filter in 28nm process P approx. 1mW



$$\left.\begin{aligned}
&V_{OUT}\left(sC_1 + sC_2\right) + g_{m2}V_{GS2} - g_{m1}V_{GS1} = sC_1V_{GS2} \\
&V_{IN} = V_{GS1} + V_{OUT} \\
&V_{GS2}sC_1 + g_{m1}V_{GS1} = V_{OUT}sC_1
\end{aligned}\right\}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{g_{m1}g_{m2}}{s^2C_1C_2 + sC_1g_{m2} + g_{m1}g_{m2}}$$

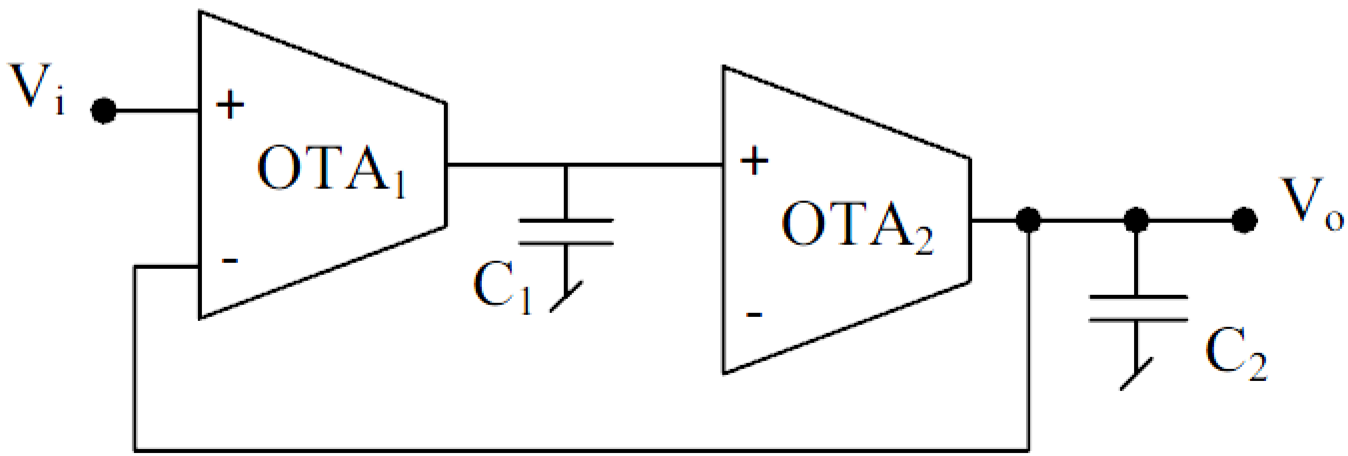
$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$$

$$Q = \sqrt{\frac{g_{m1}}{g_{\partial m2}}\frac{C_2}{C_1}}$$

A New Method to Design Multi-Standard Analog Baseband Low-Pass Filter

Ersin Alaybeyoğlu[1], Hakan Kuntman[2]

2017 10th International Conference on Electrical and Electronics Engineering (ELECO)



$$\frac{V_{LP}}{V_{in}} = \frac{g_{m1}g_{m2}}{s^2C_1C_2 + sC_1g_{m1} + g_{m1}g_{m2}}$$

$$w_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$$

$$Q = \sqrt{\frac{C_2g_{m2}}{C_1g_{m1}}}$$

10MHz – 40MHz

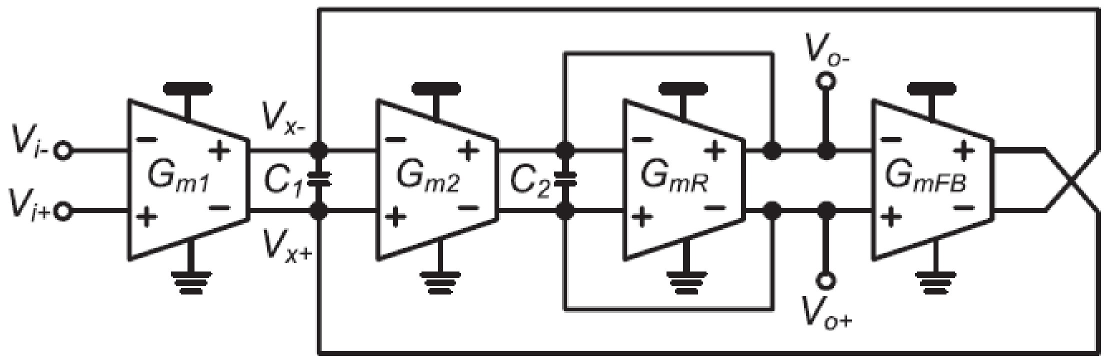
Projected Area 0.02mm^2 in 180nm proc

Low-Power *Gm−C* Filter Employing Current-Reuse Differential Difference Amplifiers

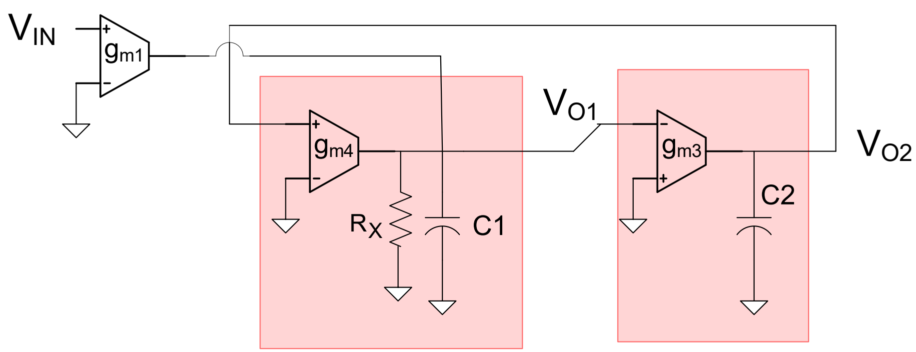
John S. Mincey, *Student Member, IEEE*, Carlos Briseno-Vidrios, *Student Member, IEEE*,
Jose Silva-Martinez, *Fellow, IEEE*, and Christopher T. Rodenbeck, *Senior Member, IEEE*

IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 64, NO. 6, JUNE 2017

Typical Differential Implementation



Typical Single-Ended Implementation



Require 4 OTAs

Current-reuse Structures

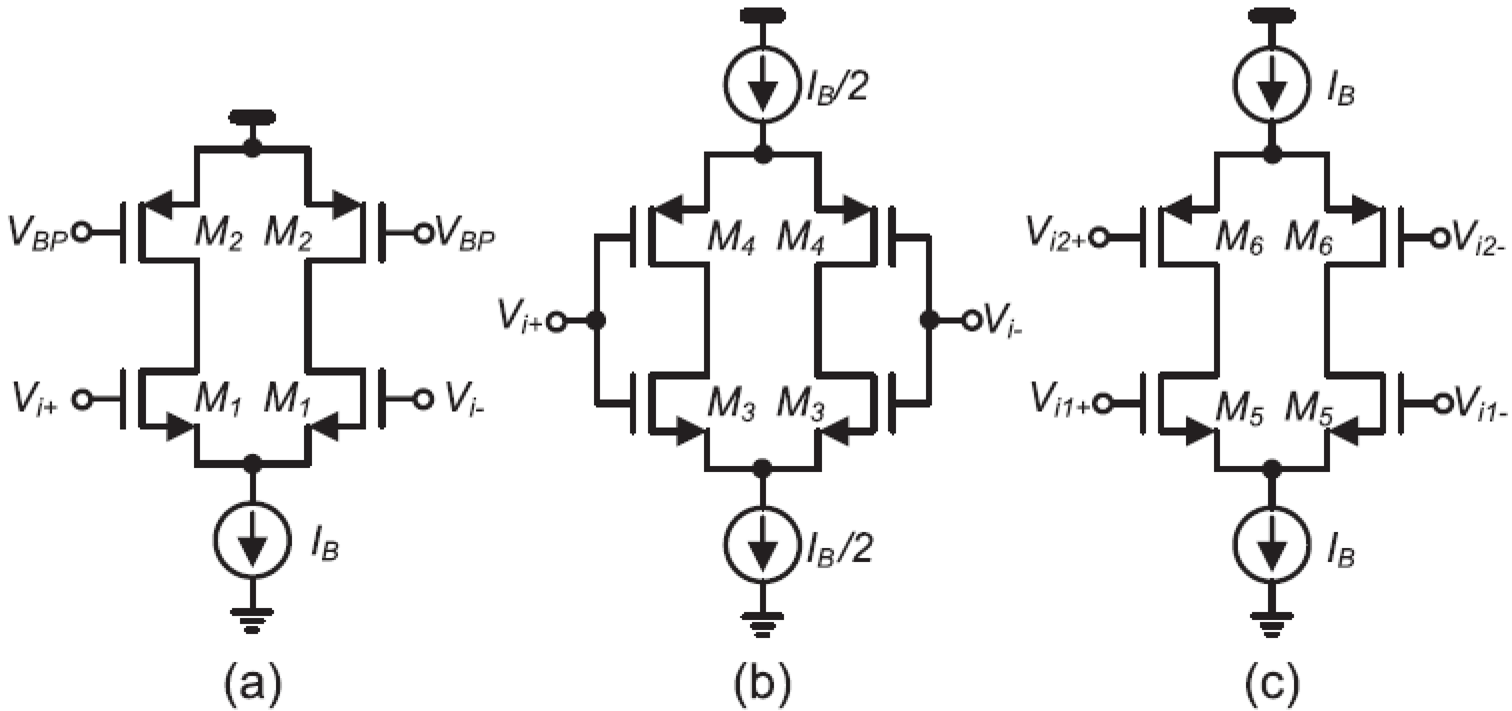
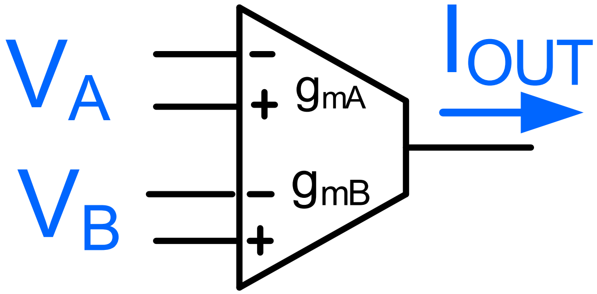


Fig. 3. (a) Conventional differential pair. (b) DDP using half the bias current. (c) Current-reuse DDA.

Dual Differential Pair: DDP
Dual Different Amplifier: DDA

Current Reuse offers potential for significant power reduction

Current-reuse Structures

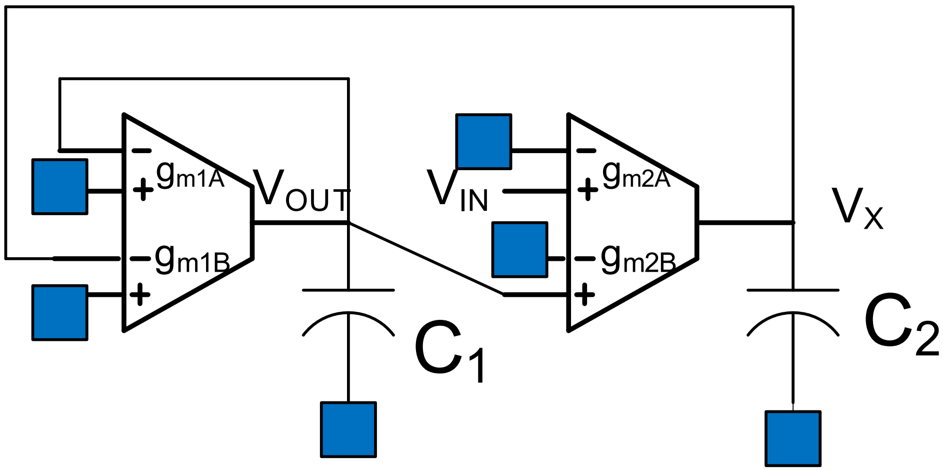


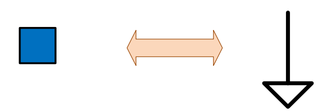
Dual input OTA

$$I_{OUT} = g_{mA} V_A + g_{mB} V_B$$

Current-reuse Structures

Consider:





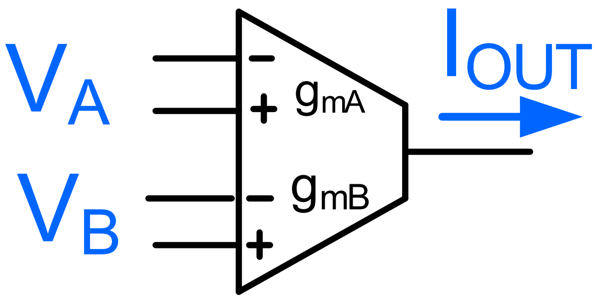
$$\left.\begin{aligned} V_{OUT} sC_1 &= -g_{m1A} V_{OUT} + g_{m1B} V_X \\ V_X sC_2 &= g_{m2B} V_{OUT} + g_{m2A} V_{IN} \end{aligned}\right\}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{g_{m2A} g_{m1B}}{\left(s^2 C_1 C_2 + sC_2 g_{m1A} + g_{m1B} g_{m2B}\right)}$$

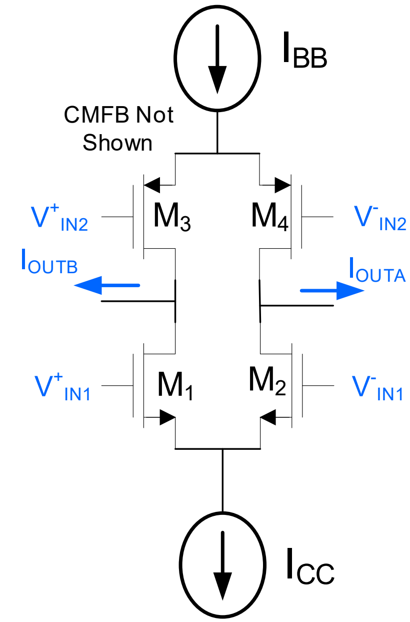
Realizes 2nd-order lowpass with just 2 OTAs

Current-reuse Structures

Dual input OTA



$$I_{OUT} = g_{mA} V_A + g_{mB} V_B$$

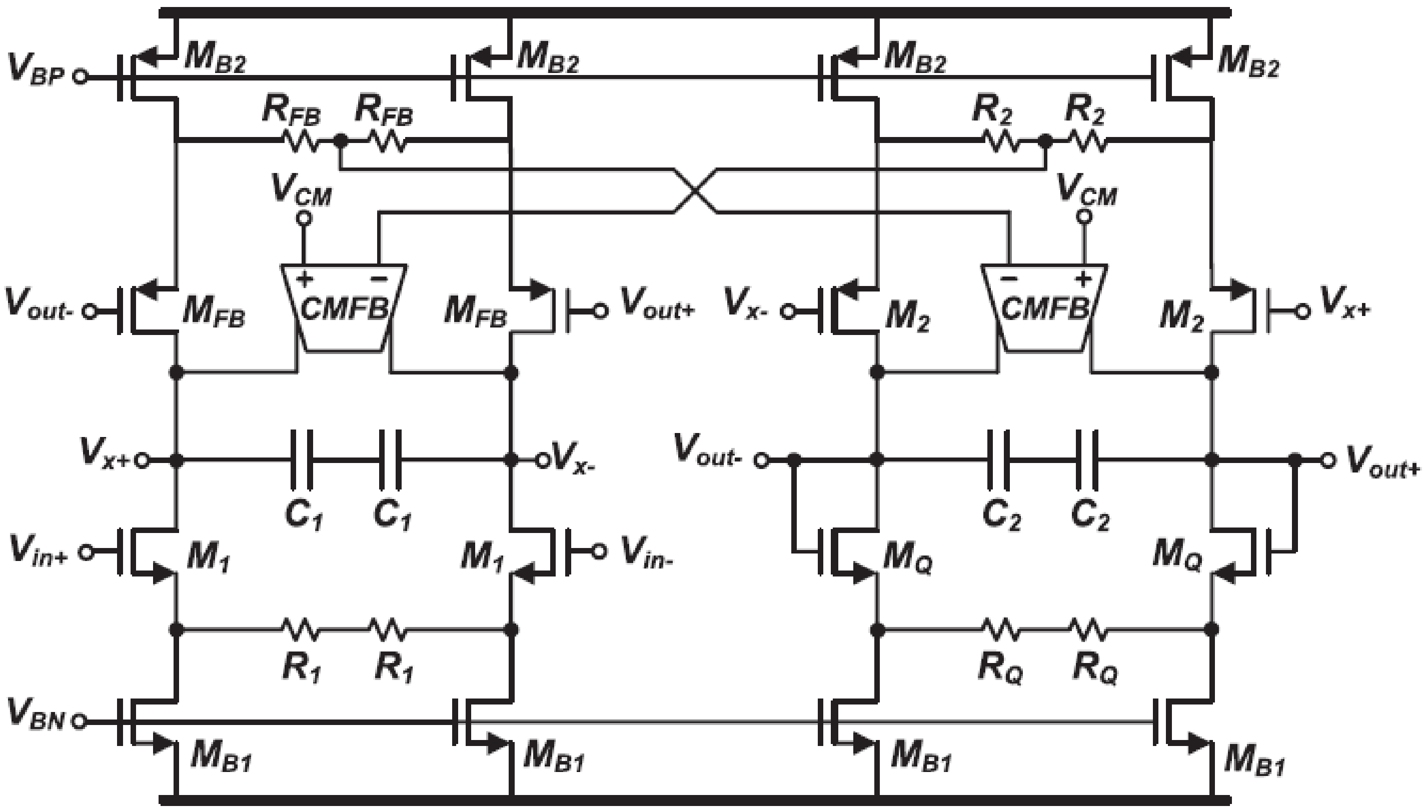


$$I_{OUTA} = g_{m2} V_{IN1}^{-} + g_{m4} V_{IN2}^{-}$$

$$I_{OUTB} = g_{m1} V_{IN1}^{+} + g_{m3} V_{IN2}^{+}$$

Current-reuse Structures

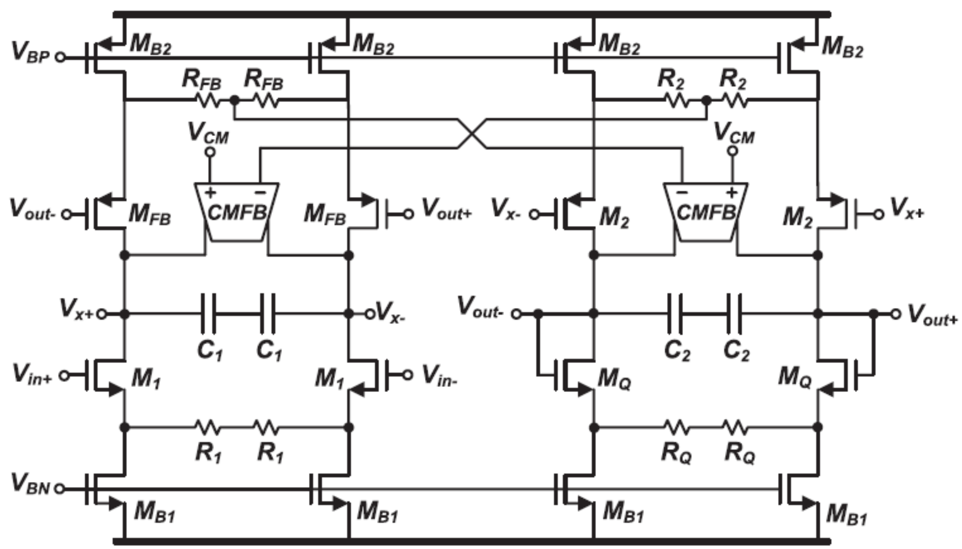
Dual input OTA



2nd Order Lowpass Biquad using Current-reuse OTA

Current-reuse Structures

Dual input OTA



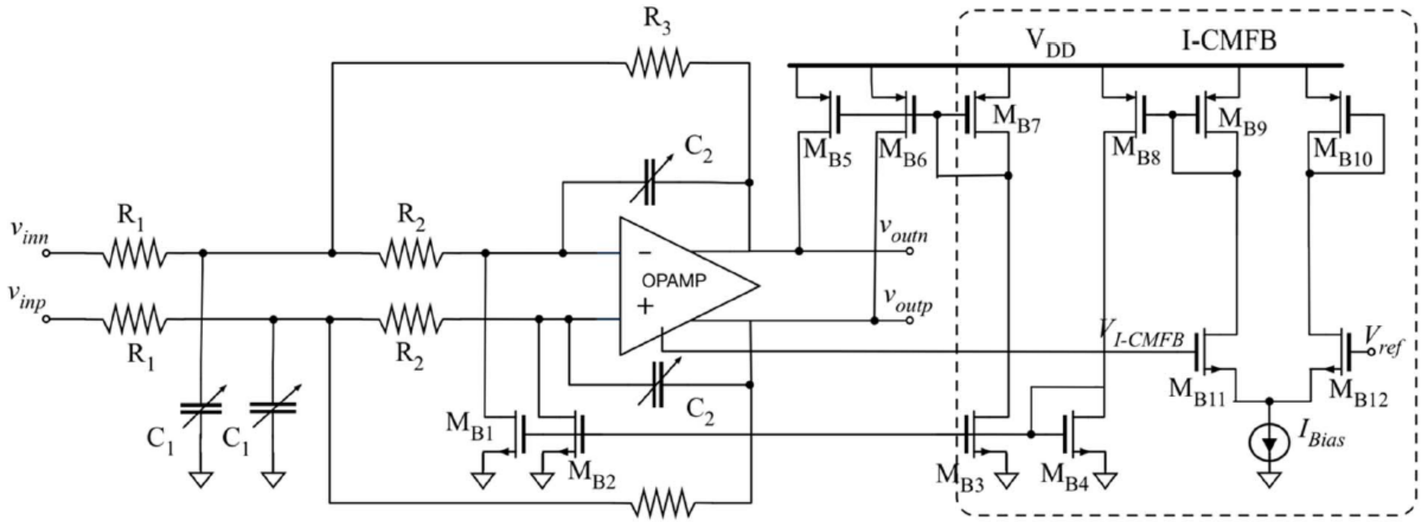
Sixth-order Butterworth G_m−C filter was fabricated

- 180-nm CMOS process
- total chip area of 0.21 mm^2
- 65MHz Band Edge
- 1.3mW/pole

A 0.9V 75MHz 2.8mW 4th-Order Analog Filter in CMOS-Bulk 28nm Technology

F. Ciciotti, M. De Matteis, and A. Baschirotto

ISCAS 2018



$$H(s) \cong -\frac{R_3}{R_1} \cdot \frac{1}{1 + sC_2\left(R_2 + R_3 + R_2\frac{R_3}{R_1}\right) + s^2 C_1 C_2 R_2 R_3}$$

$$\omega_0 = \sqrt{\frac{1}{R_2 R_3 C_1 C_2}} \qquad Q = \sqrt{\frac{C_1}{C_2}} \frac{\sqrt{R_2 R_3}}{R_2 + R_3 + \frac{R_2 R_3}{R_1}}$$

A 0.9V 75MHz 2.8mW 4th-Order Analog Filter in CMOS-Bulk 28nm Technology

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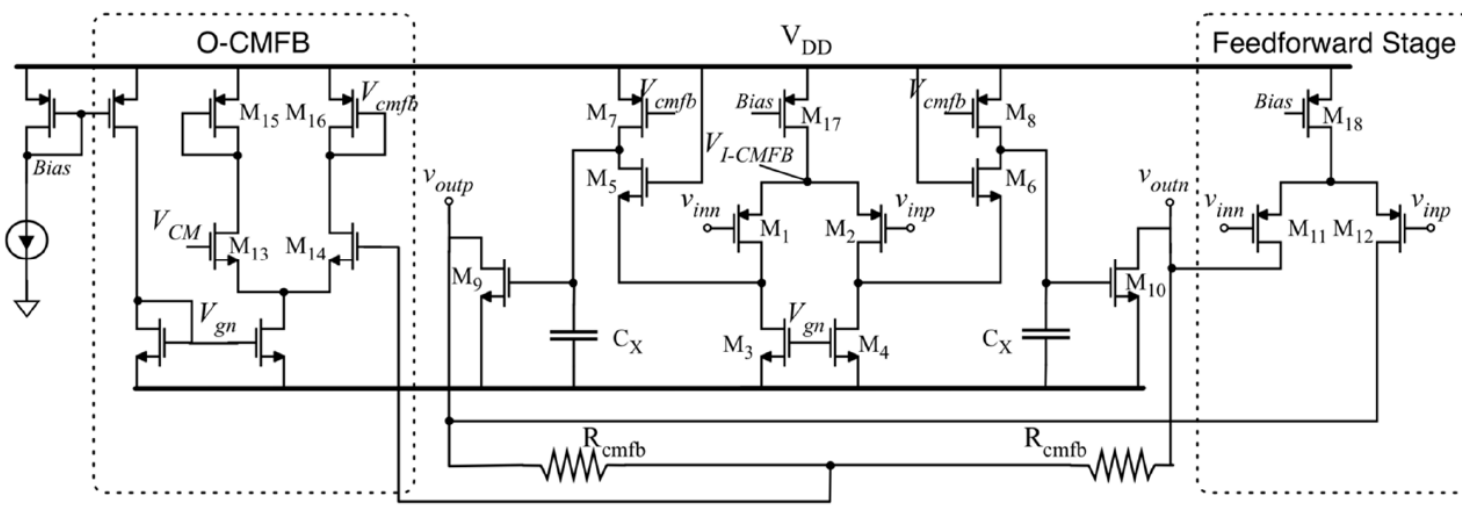

Fig. 2. Op Amp with feedforward compensation and O-CMFB circuit

CMOS 28nm process
4-bit capacitor arrays are used for frequency response programmability Filter covers the 40–105MHz range
0.7mW/pole
Area = 0.08mm^2

Stay Safe and Stay Healthy !

End of Lecture 43